PowerTeam

There is more to Verilog beyond Behavioral Simulation

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Introduction

- Behavioral Power Modeling
- Model Generation Process
- Power Simulation with Verilog
- Power Optimization Process

State of the Art

- Transistor level spice-like simulation.
- Probabilistic estimation techniques, based on toggle counts.
- RTL power simulation with approximate models.
- Power simulation by post-processing simulation results.
- Power simulation integrated into Verilog

Current Design Practice

- Functional RTL Verification,
  Primarily with Verilog,
- Followed by Synthesis and static timing verification,
- Use various transistor level tools to identify problems,
- Gate level timing simulation is losing ground.

What can be done more?

- Verilog's event queue can be used to model more than timing and behavioral changes.
- Input change $\rightarrow$ signal propagation $\rightarrow$ Output Change
- Supported by Verilog.
- Input change $\rightarrow$ Power Dissipation $\rightarrow$ Steady State
- Need to be defined.
- Can be extended to model various other phenomena.

Power Event

- E Total energy dissipated.
- t Duration of the event.
- $P = E/t$, Average power.
- Power waveform approximated by a rectangular pulse.

Power Calculation

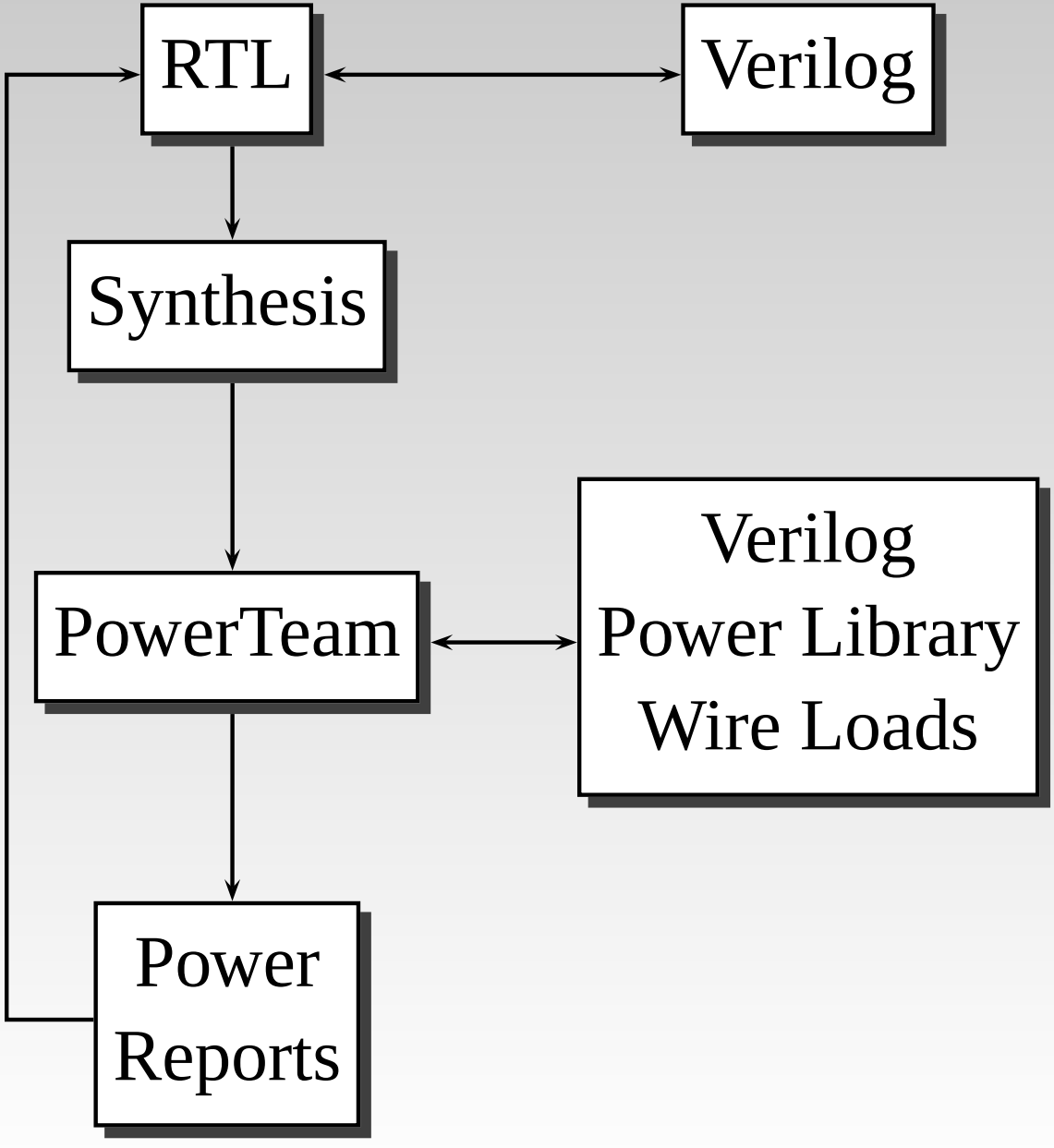
Given a netlist and its capacitive loading, Calculate

- Effective capacitive load,
- Rise/fall times,
- Signal delays,
- Energy dissipated by each path,
- Energy dissipation time,
- Power

Power Model Example

```
module inv (Z, A); output Z; input  A;
  not i0(Z,A);
  wire zd_Z; real tickDelay;
  not pow_i0(zd_Z,A);
 always @(negedge A) begin
  #(tickDelay);
  if(Z^zd_Z) $proppower({Z,zd_Z}===2'b01, 0);
 end
 always @(posedge A) begin
  #(tickDelay);
  if(Z^zd_Z) $proppower({Z,zd_Z}===2'b10, 1);
 end
 specify specparam
  phl0$A$Z = 'inv_a_lh_z_hl_power,
  plh0$A$Z = 'inv_a_hl_z_lh_power;
```

Interactive Power Optimization



How to Manage Power?

Power = $\frac{1}{2}CV^2f$

- Reduce switching rate f.
- Reduce Capacitive Load C.
- Reduce Voltage Swing V.
- Avoid Short Circuit Power.

All techniques target one or more of these objectives.

How to Manage Power?

- Design Level Optimization
  Architechtural Optimization
  Reduce Activity
  Dual Threshold, Voltage Islands
  Better Placement
- Block Level Optimization
  Adders and Multipliers
  Architechtural Optimization
  Reduce Activity
  Custom Cell Library
- Cell Library
  Better Low Power Cell Libraries

PowerTeam

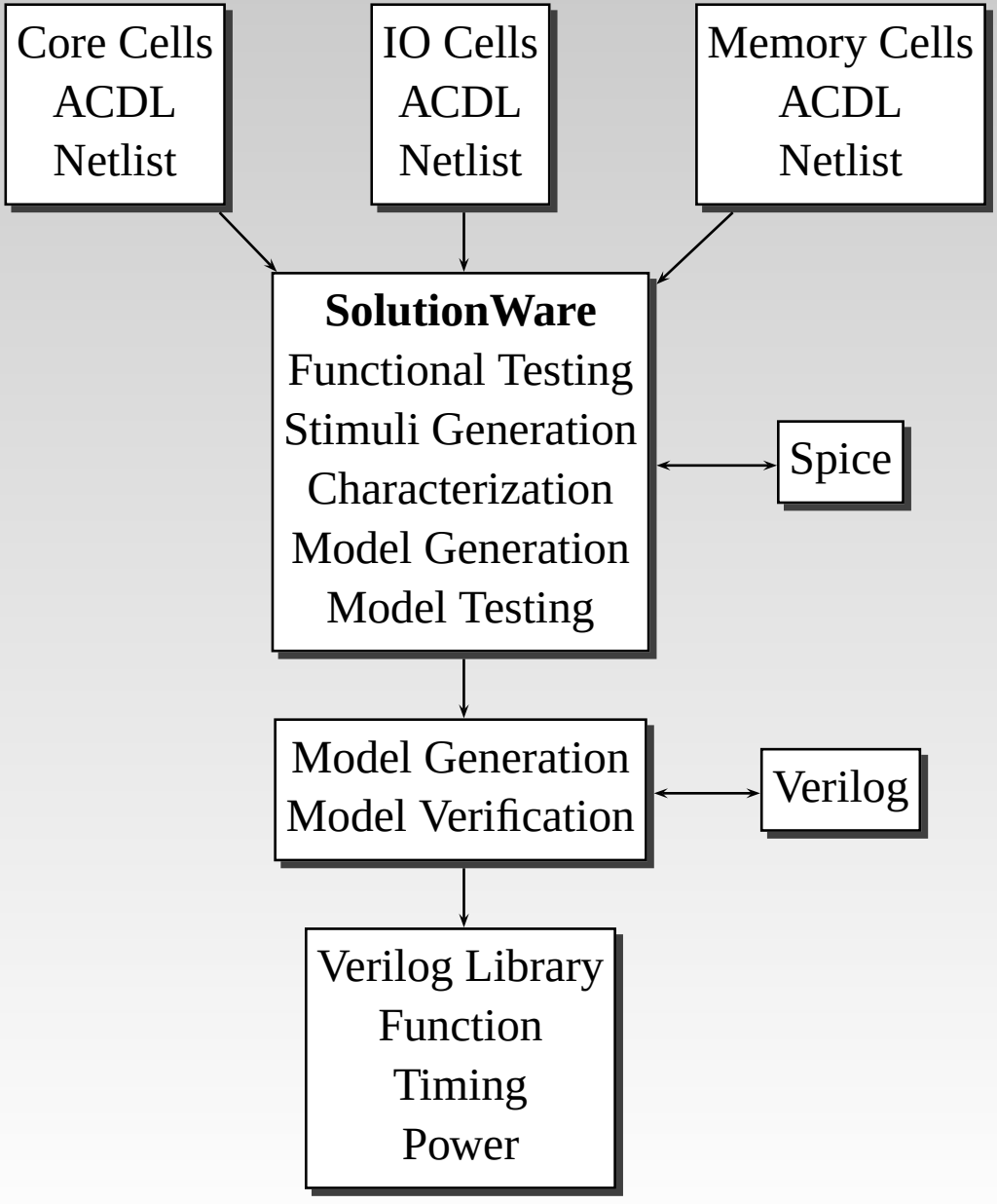
- Dynamic Power Simulator
- Integrated with Verilog, XL and VCS.
- Same user interfaces as Verilog
- Reports power and energy Use
- Integrated timing and power Simulation
- Approximately 10X slower than Timing Simulation
- Higher Speed, Accuracy, Flexibility and Capacity than any other method

Power Reports

- Instantaneous Power Use
- Total Energy Use
- Dynamic Static Power
- Capacitive Power
  Power Driven Layout Flow
- Internal Power
- Module/Instance Energy Use
  RTL-optimization
  DesignWare Components - **CellOpt**
- Cell Based Energy Use
  Library Optimization - **CellOpt**

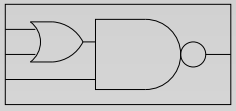
PowerTeam Reports

Power Tools - Model Generation

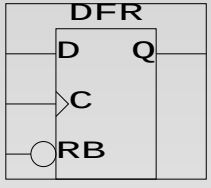


ACDL Examples

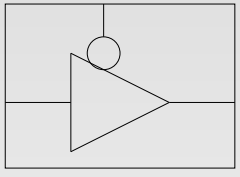
Functional Specification



O = !((A | B)&C)



Q = !RB ? 0 : rising(C) ? D : "p"



Z = GB ? "z" : A

Memory Description

```
memory.state = iq
type.iq = 2
clock.iq = CLK
chipSelect.iq = CEN
writeEnable.iq = WEN
adr.iq = A[9:0]
dataW.iq = D[7:0]
dataR.iq  = Q[7:0]
activeLow.iq=CEN,WEN
```

SolutionWare - Run Times

- Fast Setup/hold algorithm
- Approximately 65 hours, 400 cells, 7x7 tables, timing, power, Sunblade 1000/600 with Athlon 3000+ Linux PC, lumped caps
- Scan flop with sync reset, 3 hours, 26 setup/hold, cross caps
- NAND2 2 minutes, cross caps
- Simple Flop 18 minutes, 4 setup/hold, cross caps.

Conclusions

- Verilog is capable of power simulation.
- Can generate actionable power reports.
- Verilog is a good vehicle for analyzing all event driven phenomena.