The Predictive Analysis Company

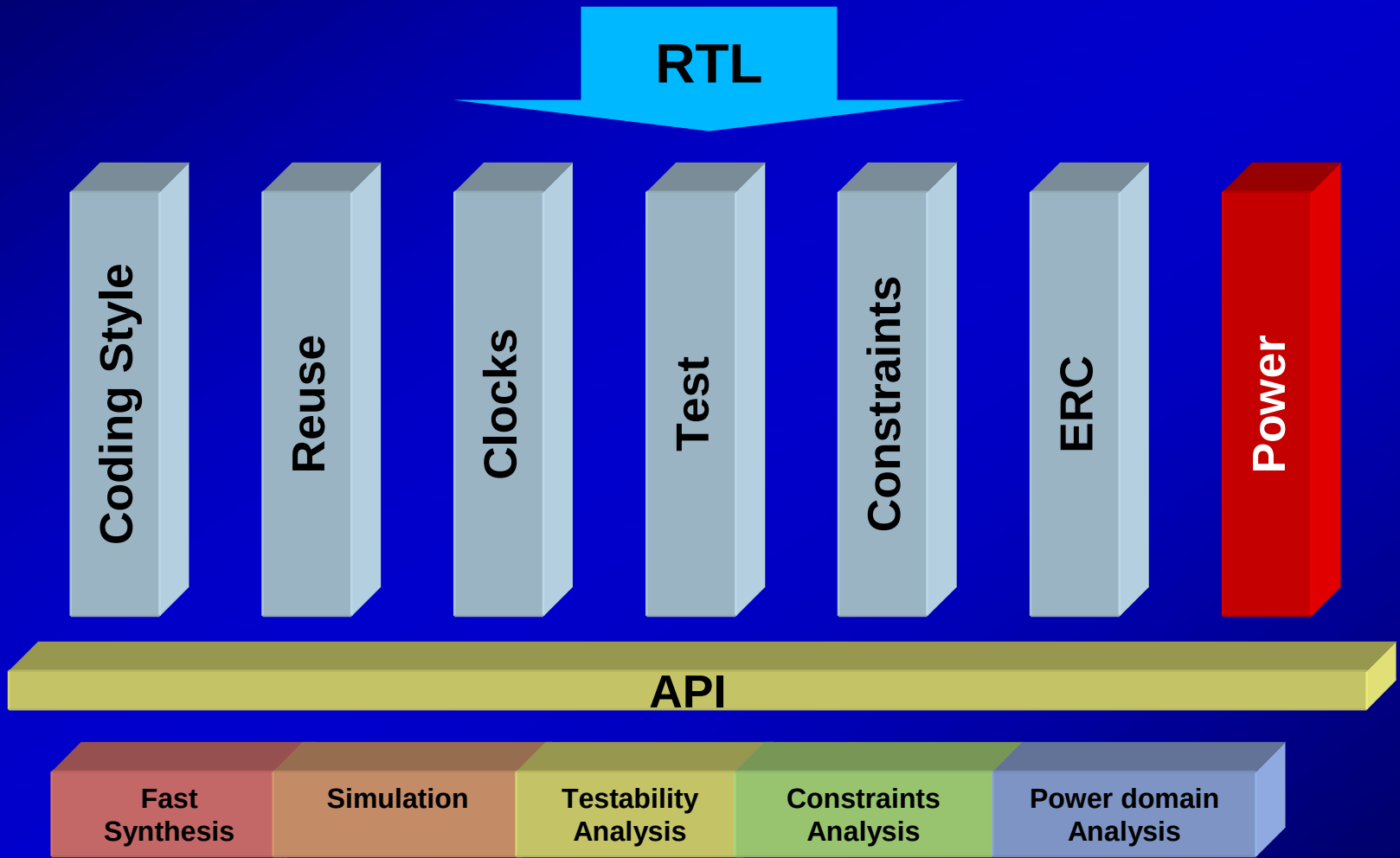
Policy-Based Approach to Guiding Low Power Design Methodology

EDP 2004, Monterey, CA
April 26, 2004

Agenda

- Power consumption is a critical issue in semiconductor design
- Current approaches to low power design
- Low power design methodology
- Presenting a new approach to detecting and fixing low power design issues early in the design cycle

Technology Driven Predictive Analysis



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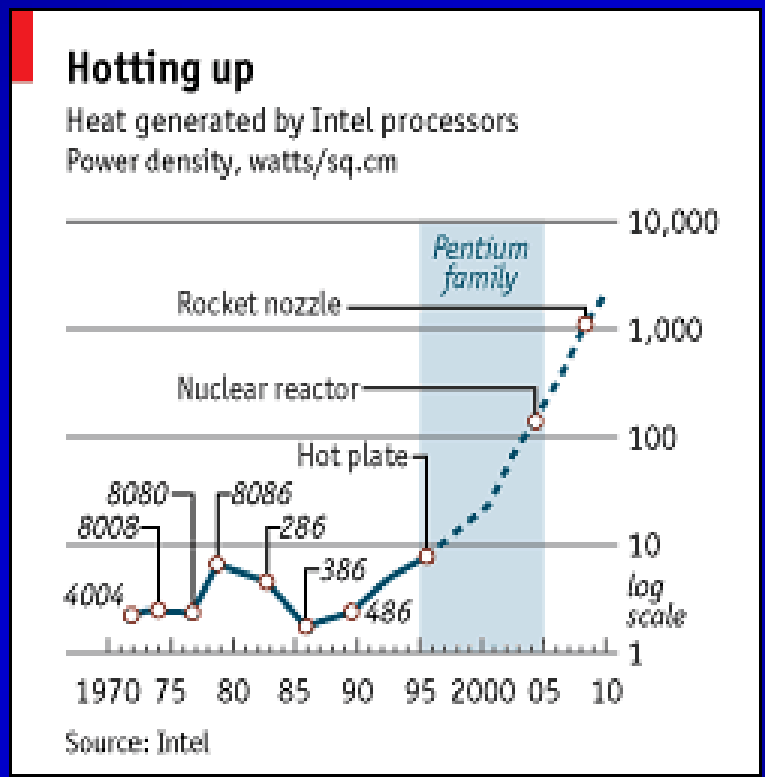
Crisis of Power



Economist: March 13, 2003

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Low Power Drivers

- Design Feasibility
- Cost → Packaging determined by power density
  - All applications
  - Cable Modems
  - Set Top Boxes etc

- Product Differentiation → Battery Life
  - Cell Phones
  - PDAs
  - MP3 Players

- Reliability and Signal Integrity Issues

Power Dissipation

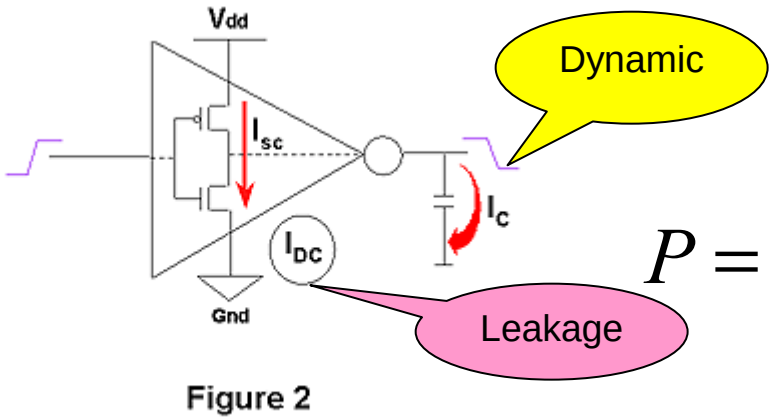

Figure 2

Dynamic

Leakage

$$P = \alpha \cdot C \cdot V^2 f + Leakage$$

Activity

Voltage

Frequency

Capacitance

- Voltage Scaling
- Power Domains and Leakage
- Clock Gating
- Some Additional Options

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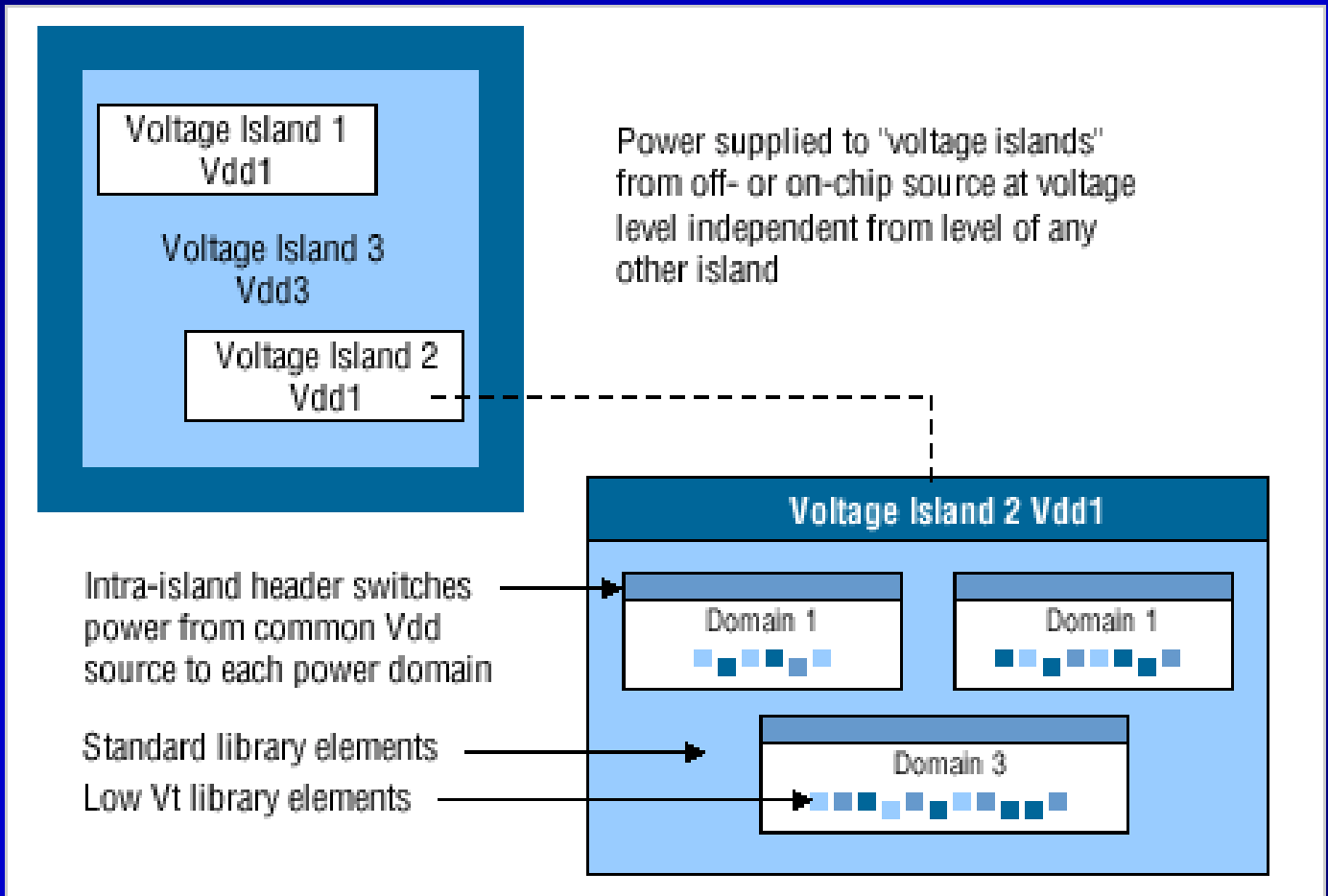
Not a solved problem

- Dynamic Power
  - Voltage management using multiple voltage domains
  - Activity Reduction techniques -- Clock gating
- Leakage Power
  - Leakage is increasing rapidly with advancing technology
  - Voltage management through shut down – Power domains
- Introduces unique design methodology challenges
  - RTL lacks voltage information
  - Voltage, power, gated clock domains lead to complex design issues
  - Changes made late in the design cycle may lead to re-spin

Low Power Design Requirements

- Address low power issues early in the design cycle
- Ensure adherence to best low power practices
- Deploy custom low power methodology across project/company

Voltage Management: IBM Cu8



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Voltage Scaling

- How to maintain throughput under reduced supply?
- Introducing more parallelism/pipelining
  - Area increase – cost up
  - Cost/power tradeoff
- Multiple voltage domains
  - Separate supply voltages for different blocks
  - Lower VDD for slower blocks
  - Cost of DC-DC converters
- Dynamic voltage scaling – with variable throughput
- Reducing V_{TH} to improve speed
  - Leakage issues, multi-threshold and shut-down solutions

Voltage Domains

- Power reduction using multiple voltage domains
  - Only critical portions of design at higher voltage
  - 25% at Vdd and 75% at 0.6-0.7 Vdd
  - 45-50% lower dynamic power
- Design challenges – e.g, Correct level shifters on all crossings

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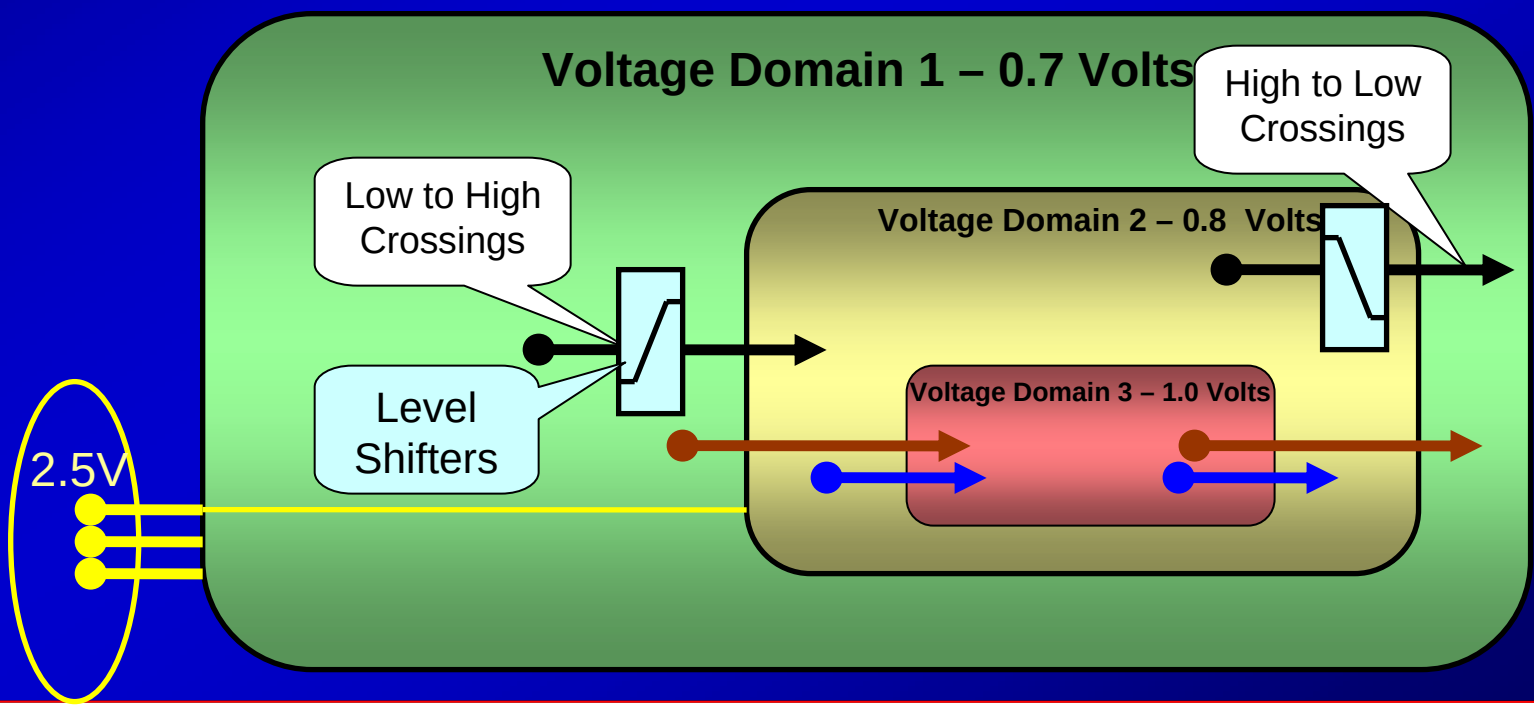

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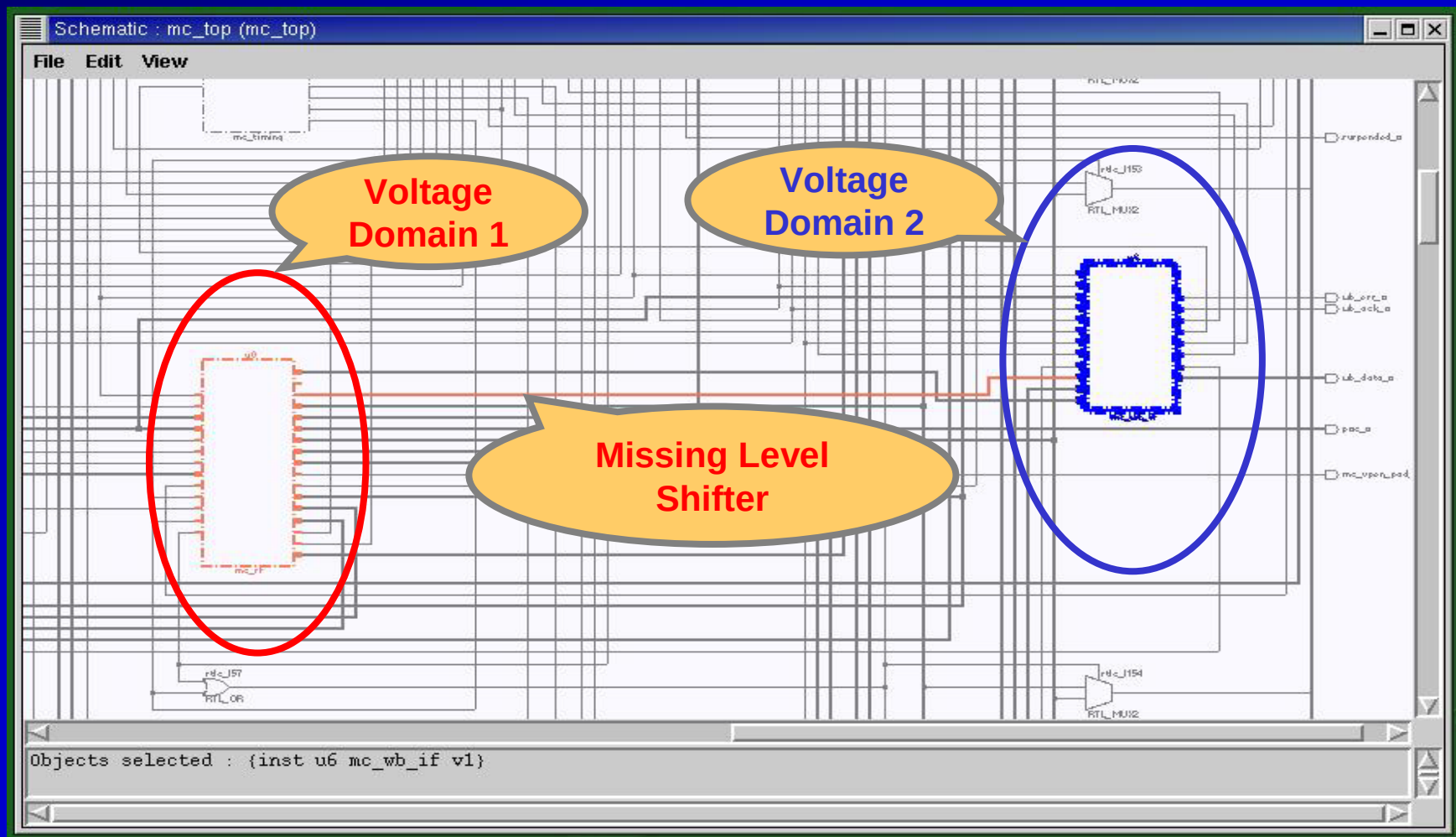
Voltage Domains



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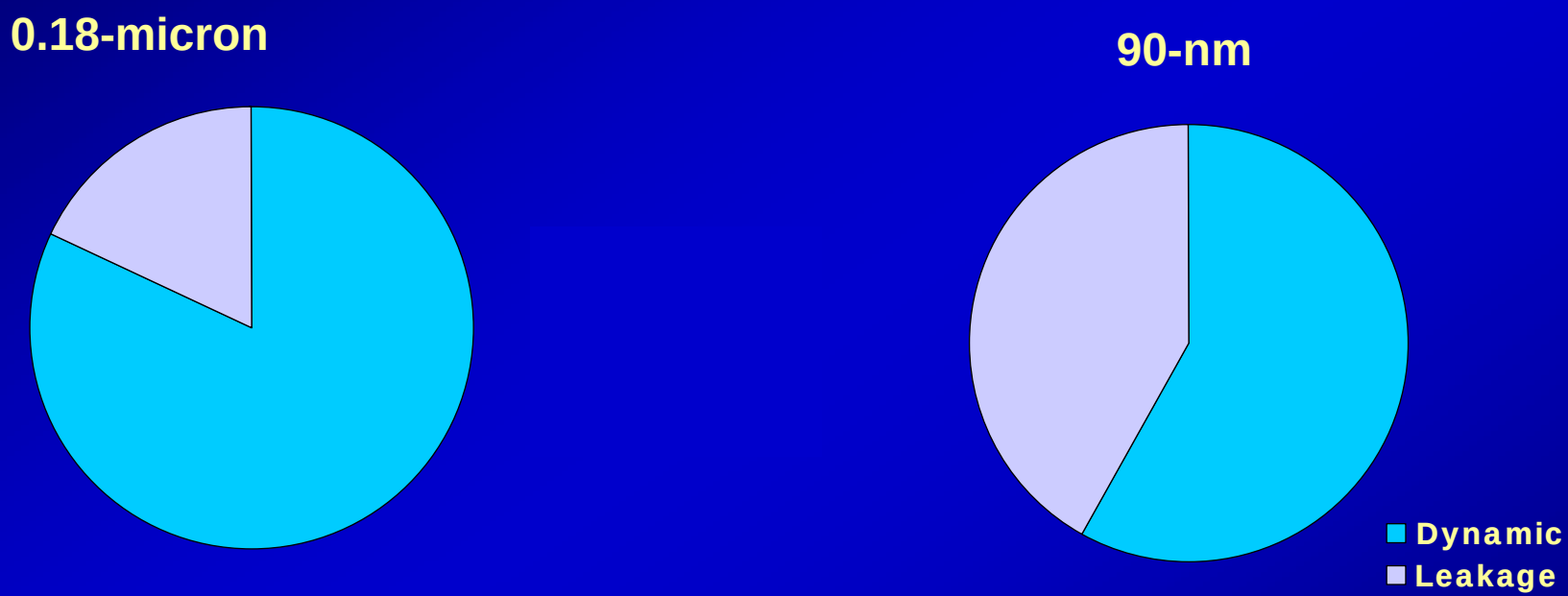
Increased Leakage



- Leakage becoming a major portion of total power consumption
- Currently 10-20%, ~40% for 90nm, and higher in future technologies
- Shutting down portions of the design to deal with standby leakage
- Standby more important for application such as cell-phone

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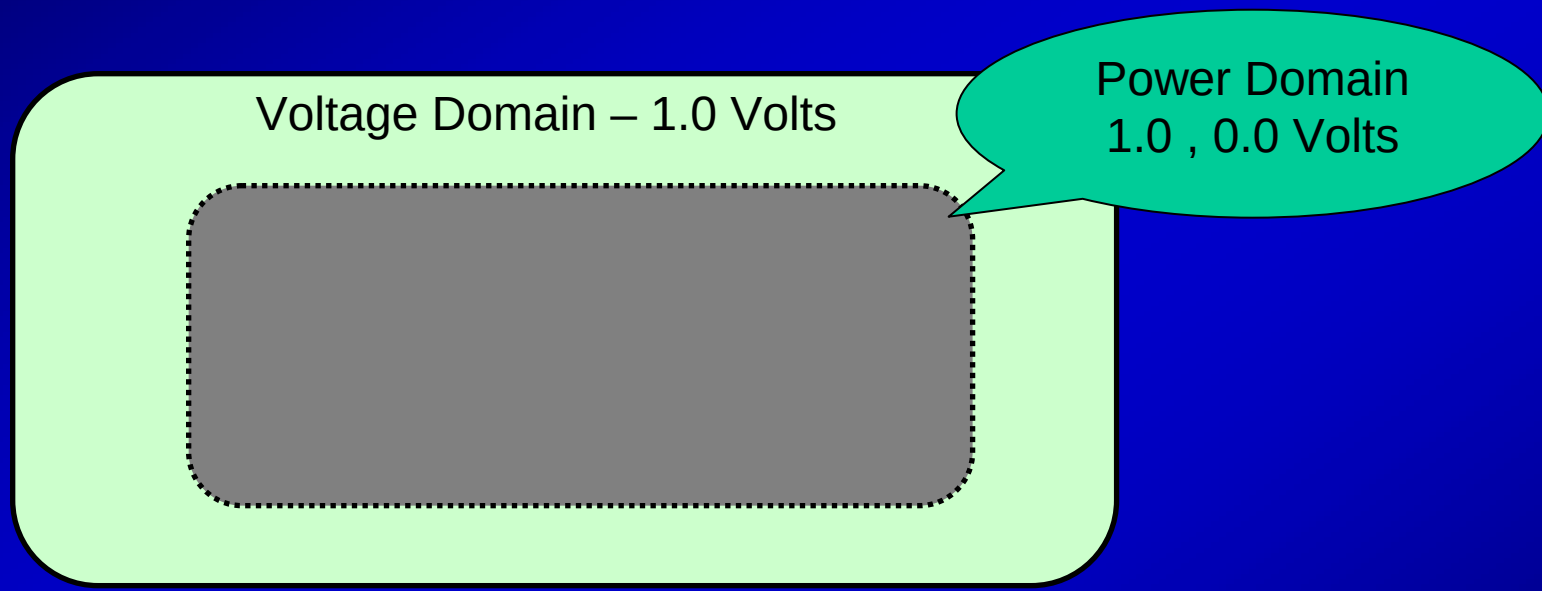
Power Domains



Shutting down large portions of design in the stand by mode

- Many blocks on a chip are not used all of the time
- Power to these blocks can be turned on and off as needed
- Specialized blocks for I/O devices and graphics.
- PowerPC 405LP shuts off portions of the chip that are not in use
  - Reducing active and standby power by up to 10 times compared with current designs

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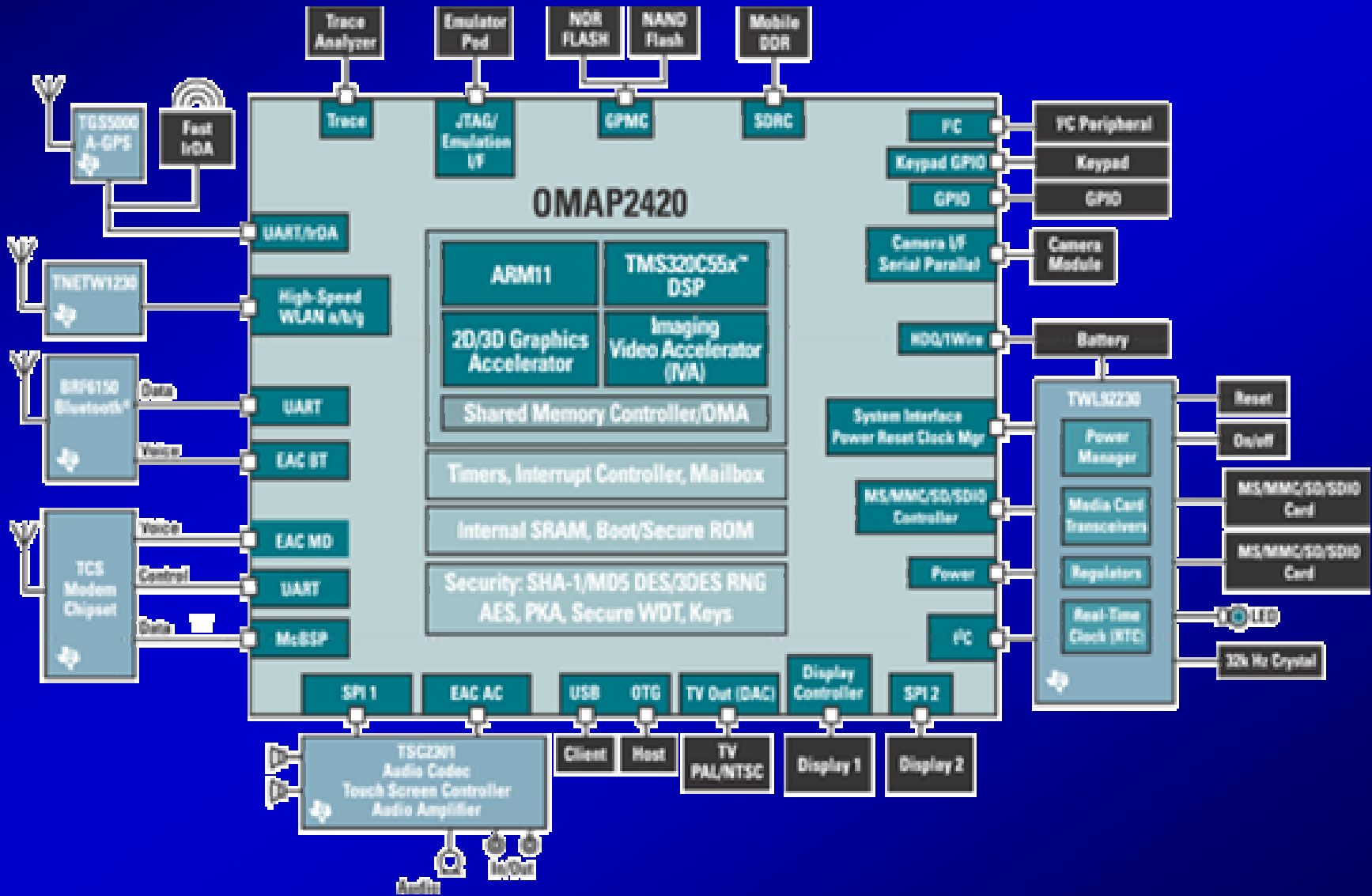
Complex SoCs for Multimedia



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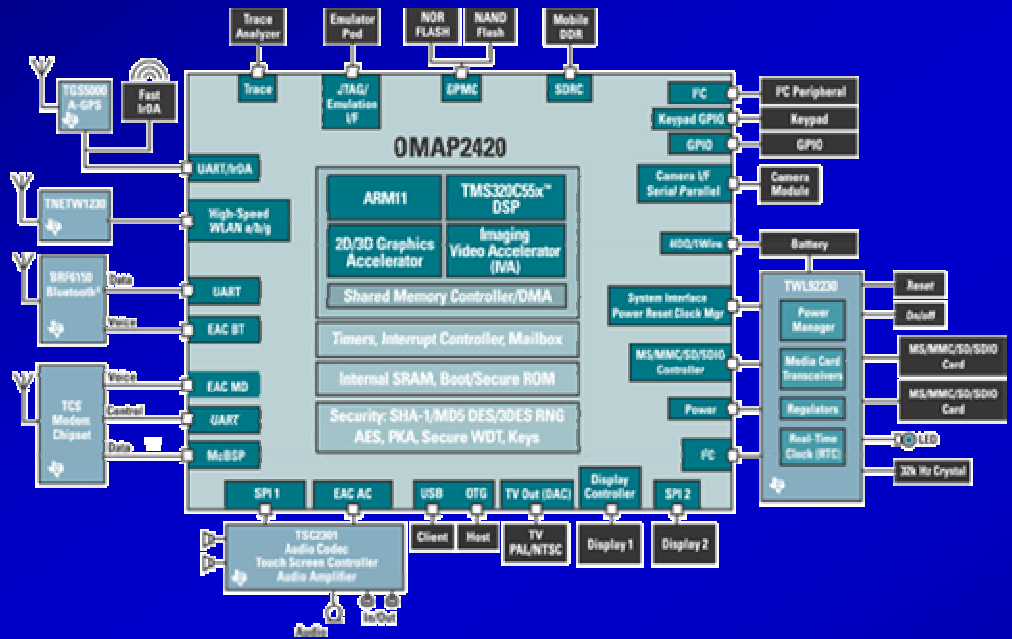
Complex SoC-Usage Scenarios



- OMAP2420 includes an ARM, a DSP, 2D/3D graphics accelerator, imaging video accelerators, high speed interconnects and many peripherals on a chip
- Many modes of operation, many power management modes
- Multiple voltage domains, power domains, large number of gated clocks etc

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Power Domains

- Leakage power becoming a major concern
  - Leakage power ~40% for 90nm technology
  - And increasing in future process technologies
  - Shut down portions of the design to reduce leakage
- Design challenges – e.g., Ensure proper isolation of signals

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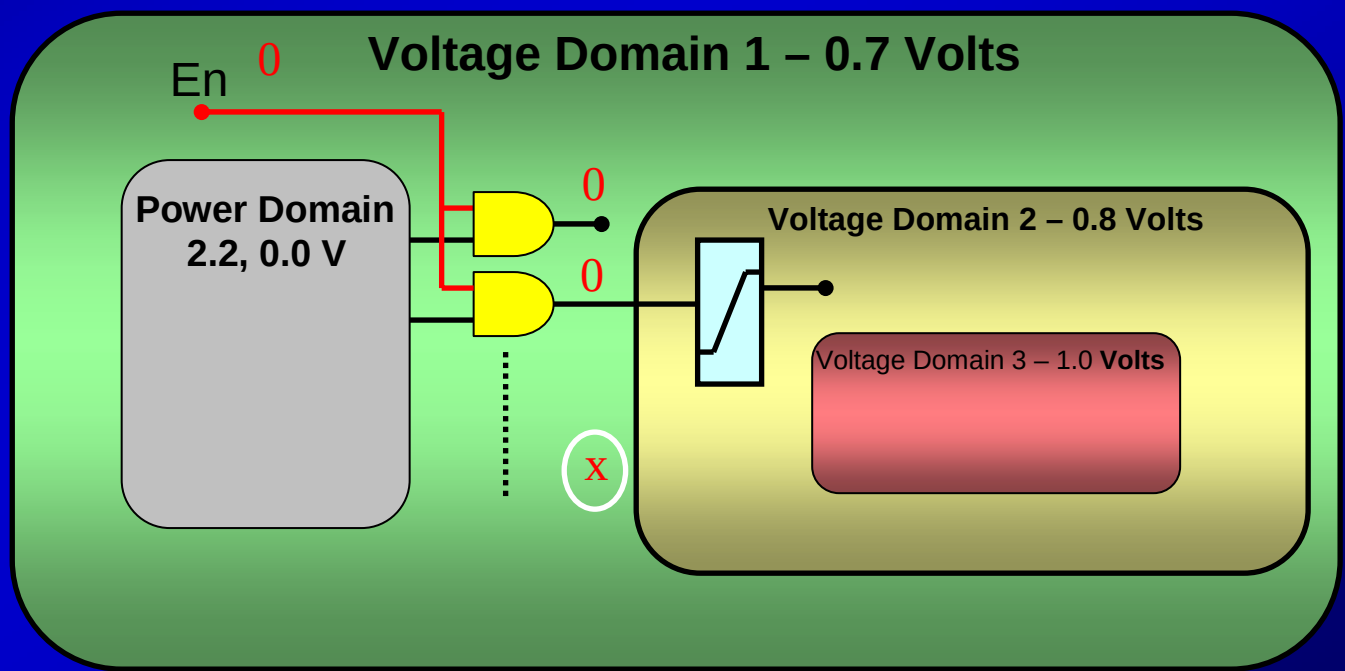

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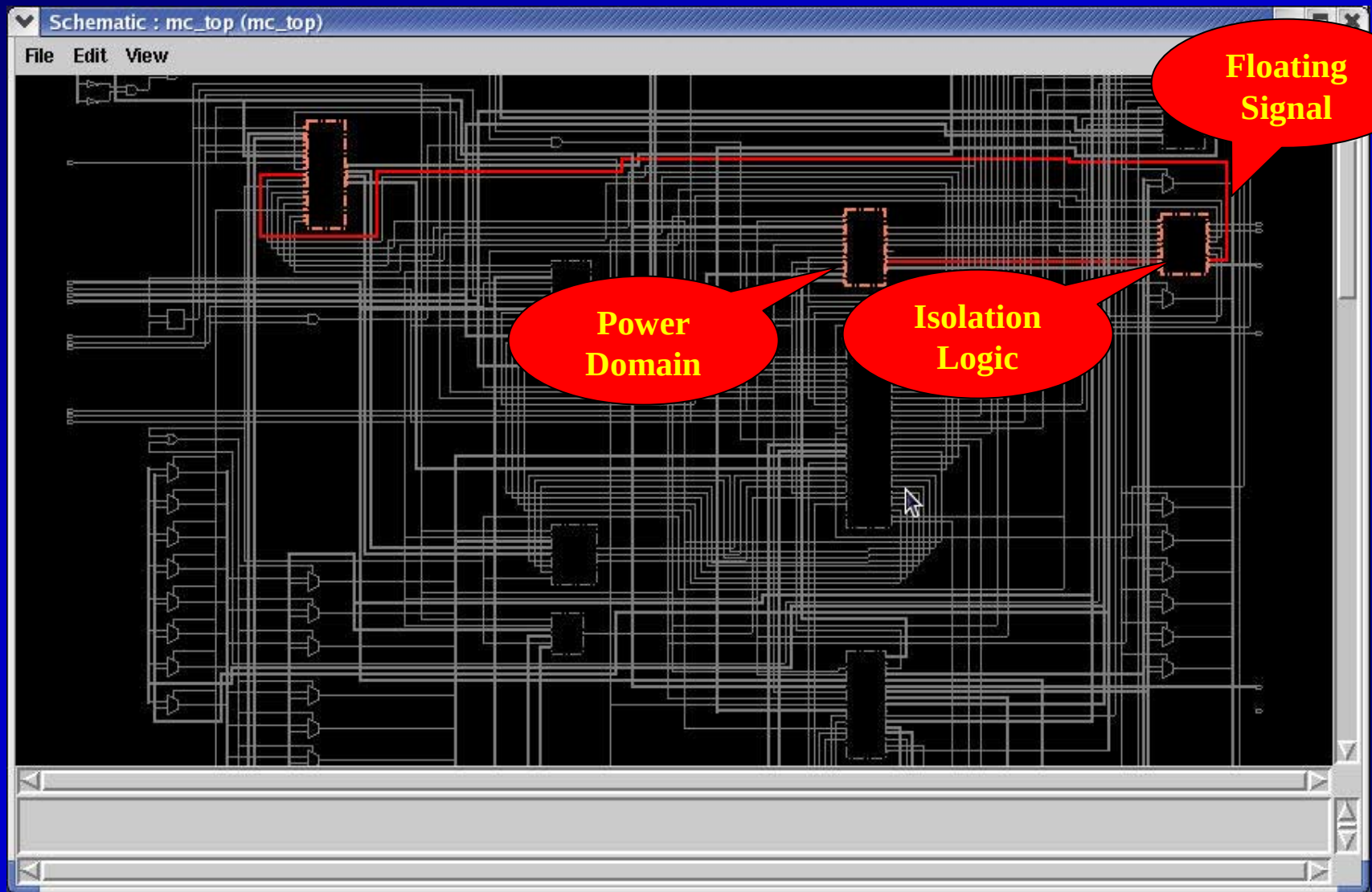
Floating Signals



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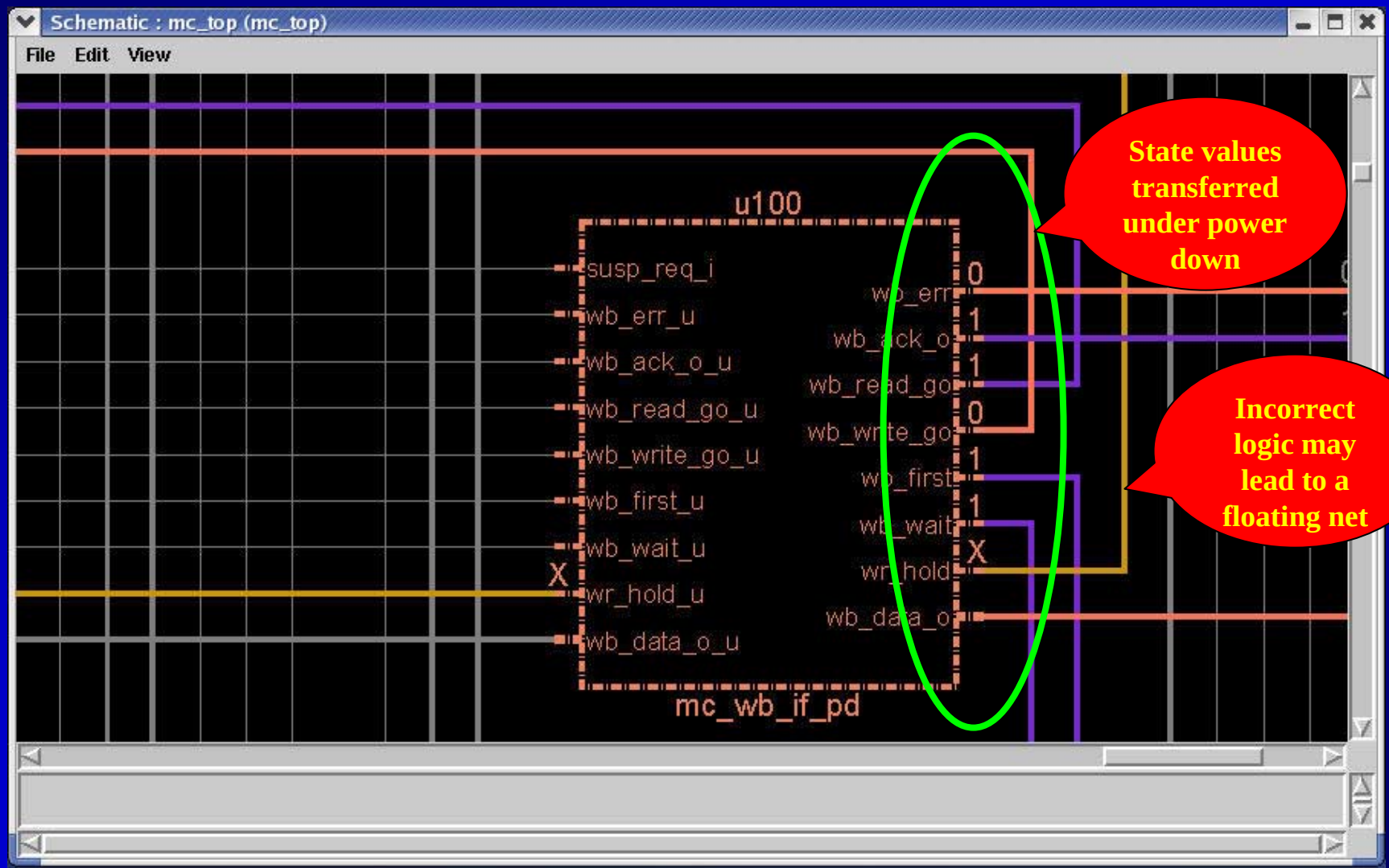
Analyzing Power Domains



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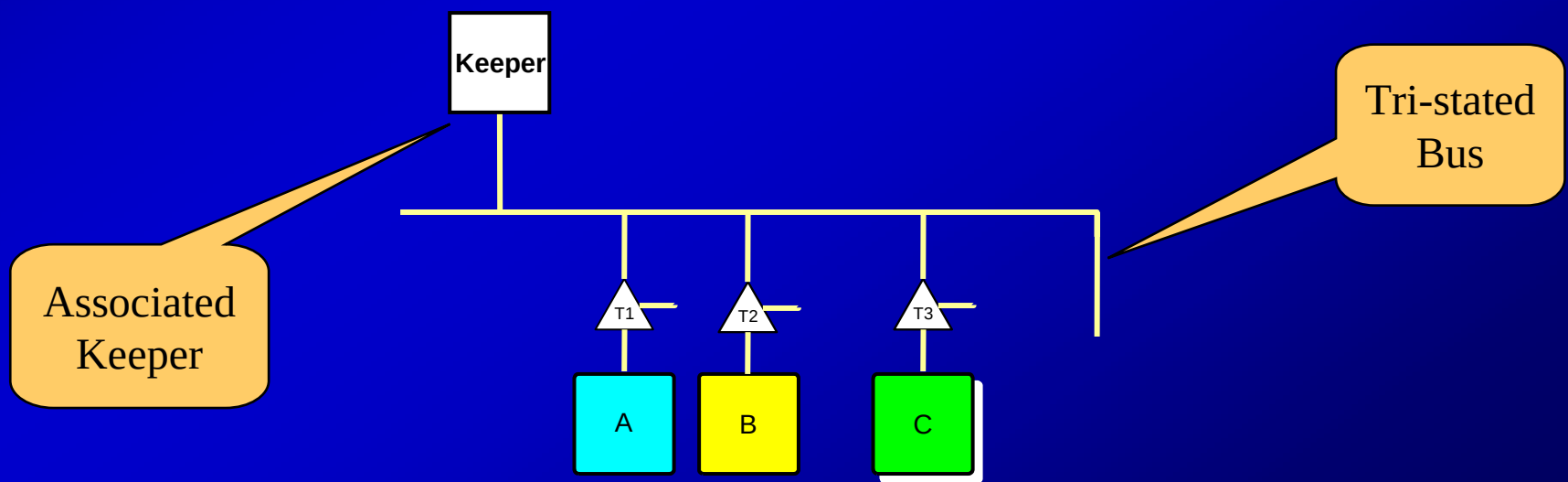
Clock Gating

- Clock gating is a key technique for activity reduction
  - Partly designer (knowledge) driven, partly automated
  - Requires analysis of existing gated clock domains
  - Efficient introduction of additional gated clocks is important
- SpyGlass LP looks across modules to find larger sets of flops where conditions exist for clock gating
- Spyglass LP identifies back-to-back gating situations
- Spyglass LP highlights possible sharing of gated clocks

Bus Issues

- Problem:
  - Buses can have large parasitics associated with them
  - Buses can be left floating and consume leakage power
- SpyGlass Solution:
  - Identify and provide information on buses
  - Ensure special bus drivers and receivers are in place
  - Ensure tri-stated buses are not left floating



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Best Practices for LP

- Bus Guidelines
  - Identify and provide information on buses
  - Ensure special bus drivers and receivers are used
  - Ensure tri-stated buses are not used or not left floating
- Techniques for datapath elements
  - Ensure selectively used datapath units are latched
  - Identify pre-computation candidates
- FSM Guidelines
  - Ensure optimal encoding (one-hot, gray, min bits)
  - Identify dead, and redundant states
  - FSM Viewer -- Extracts STG from RTL

Customization

- Every engineering team has their own rules for low power design
  - Proprietary rules that reflect collective experience and expertise
- Enables customization of specific design methodology low power rules
- Examples
  - Rules for design methodology around power domains for leakage reduction
  - Clock gating design methodology
  - Specific guidelines for 90nm and 65nm design methodology needs [multiple voltage/power domains]

Summary

- Addresses low power design techniques which have maximum impact on power
  - Power Domains
  - Voltage Domains
  - Clock Gating
- Customization enables rapid development and deployment of customer specific rules
- High capacity enables full-chip analysis