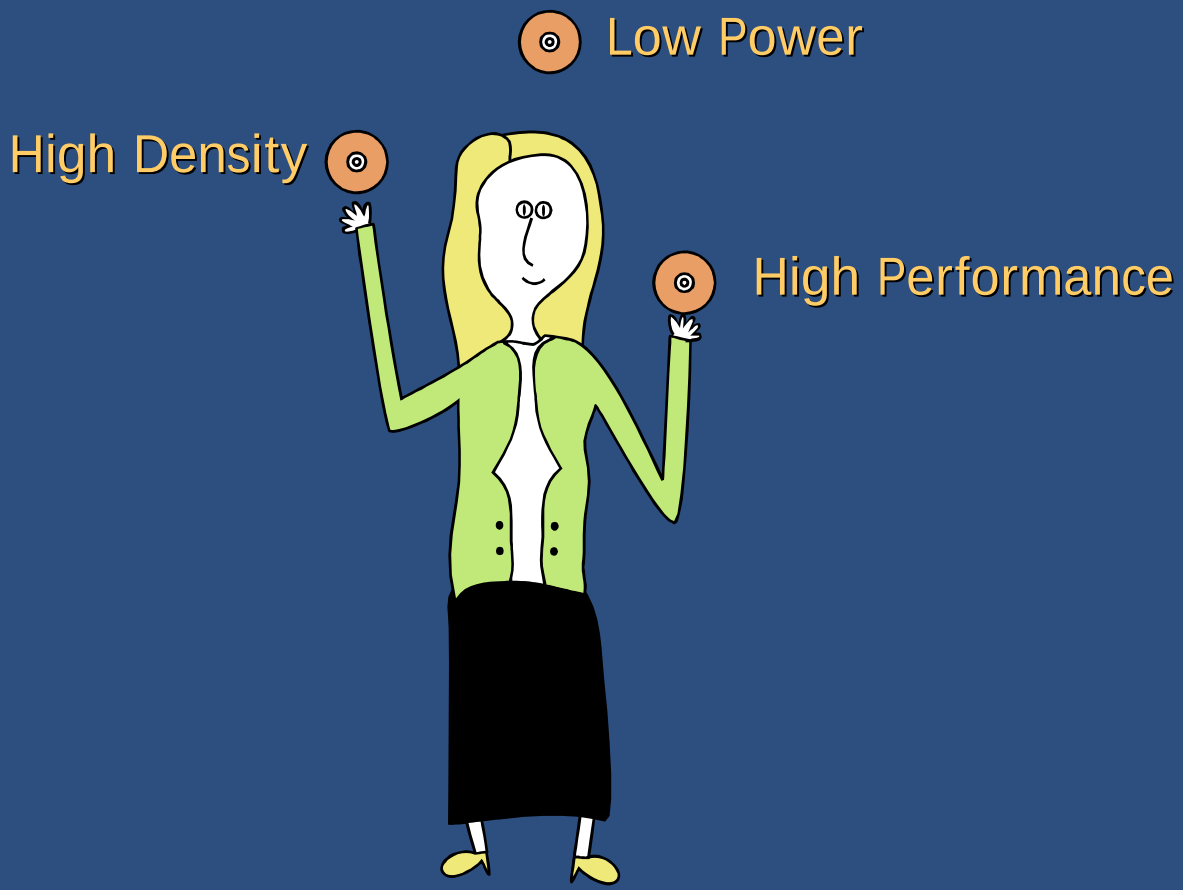
ORINOCO®
SAVES POWER!

chipvision
Design Systems

ChipVision Design Systems

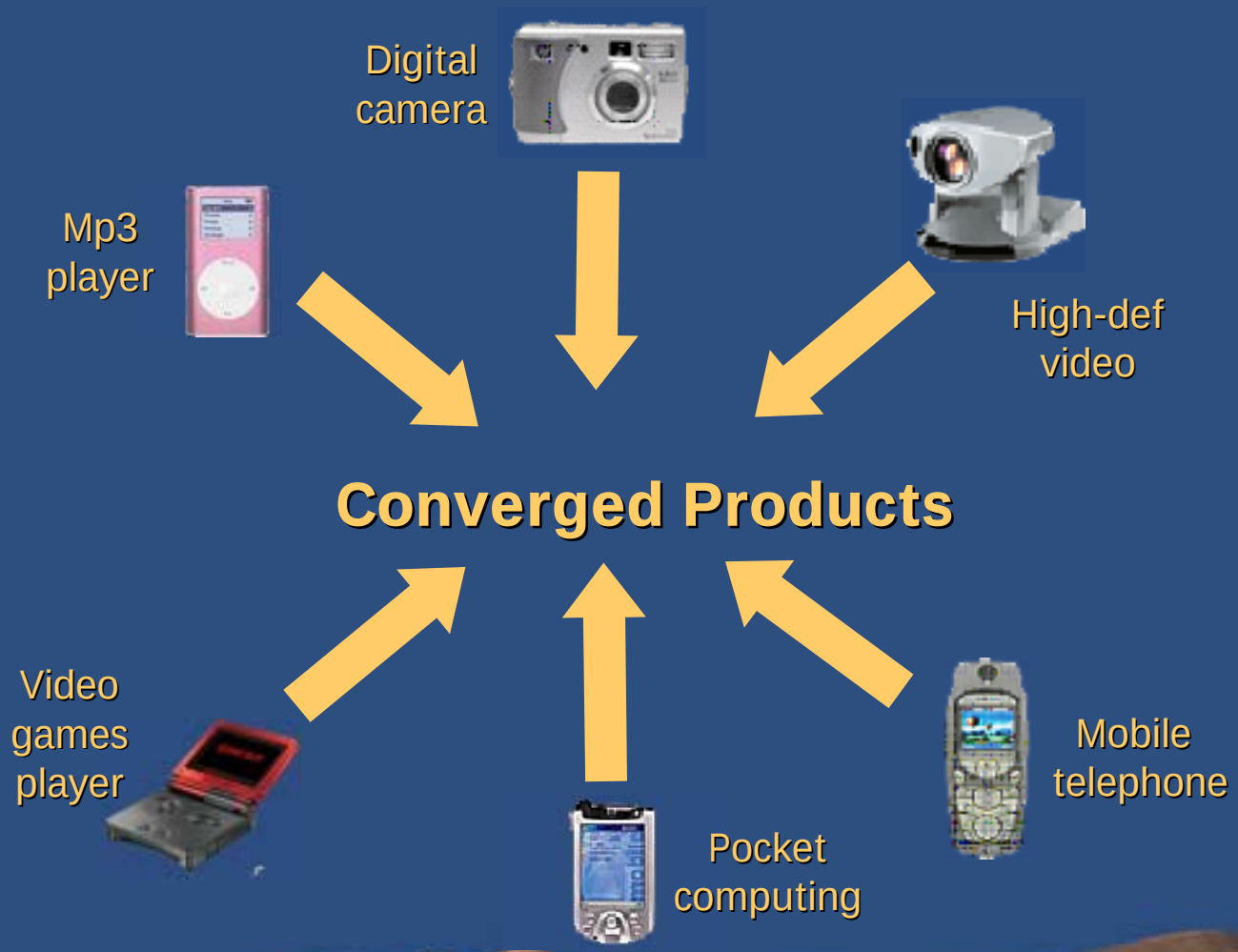
Stan Krolikoski
CEO

Multiple Demands on Today's IC Designers



It's Not Just About Size and Speed Any More!

Battery Life Becomes An Issue At 135nm



At 90nm Power Is An Issue Everywhere

Data Processing

Data Storage

Military/ Aerospace

Industrial Electronics

Automotive

Consumer Electronics

Wireless Communications

Wired Communications

EDA Has Focused on Low-Level Power Analysis

Architecture

ChipVision, PowerEscape, ASC
- PowerEscape complementary to ORINOCO
- ASC seems to only have research tool

RT-Level

Sequence, Synopsys, Cadence, Atrenta, Veritools

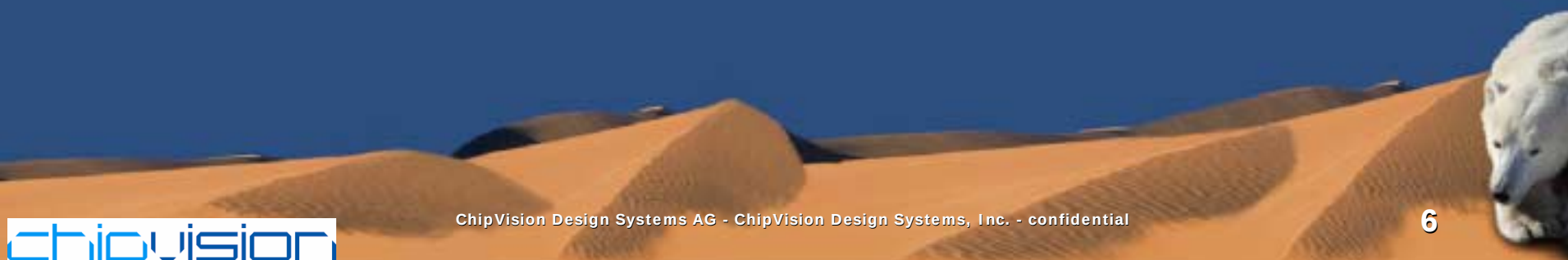
Gate/Xstr-Level

Synopsys, Cadence, Magma, Mentor, …
- The bulk of EDA Power Tools

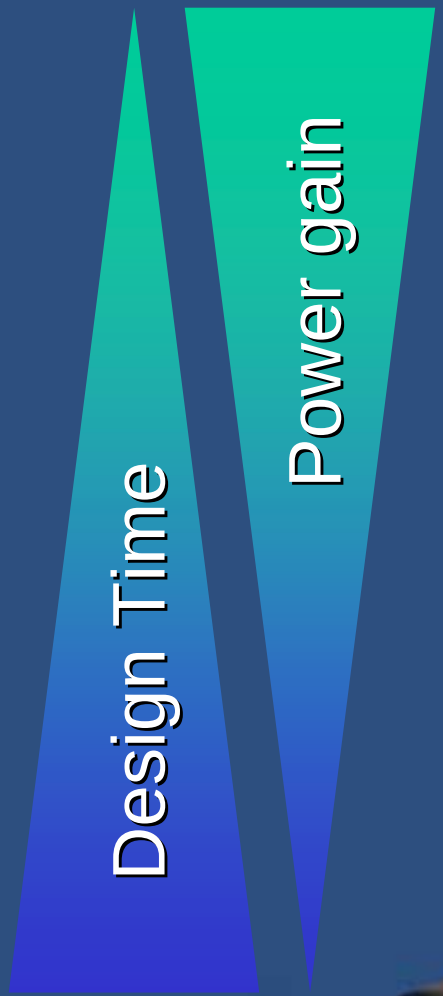
But The System Level Must Be Addressed

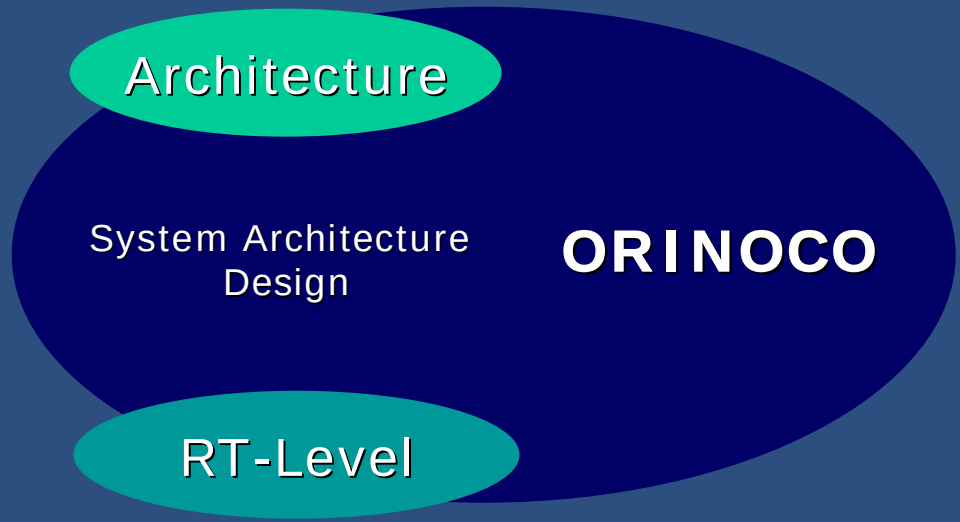
"For Continued Improvement in Designer Productivity, an emerging system-level of design, well above RTL, is required"

International Technology Roadmap for Semiconductors, 2003 Edition-- Design, p. 9



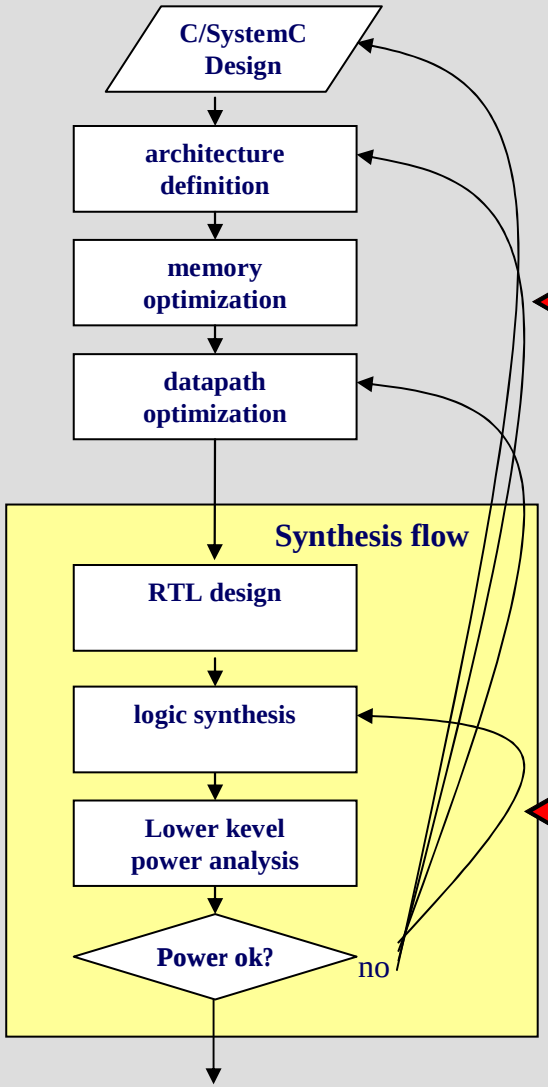
Attacking Power at The System Level





Gate/Xstr-Level

Design Flow Without ORINOCO®



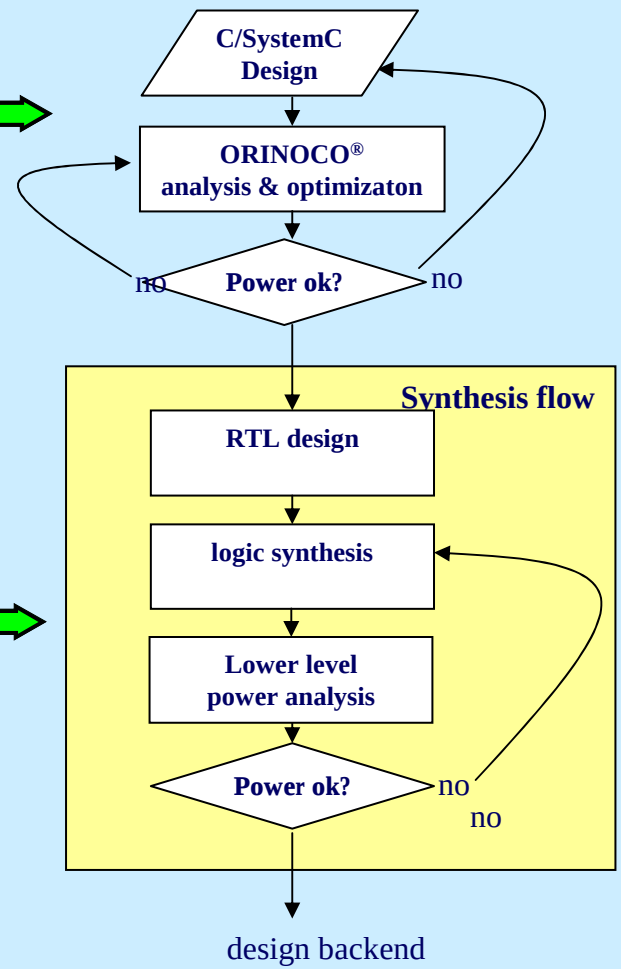
With ORINOCO
Architects solve many power issues up-front.

Without ORINOCO
Missed power budgets lead to costly respins.

With ORINOCO
Fewer power issues to solve at lower levels.

Without ORINOCO
All power problems analyzed at lower levels– very inefficient!

ORINOCO-based design flow



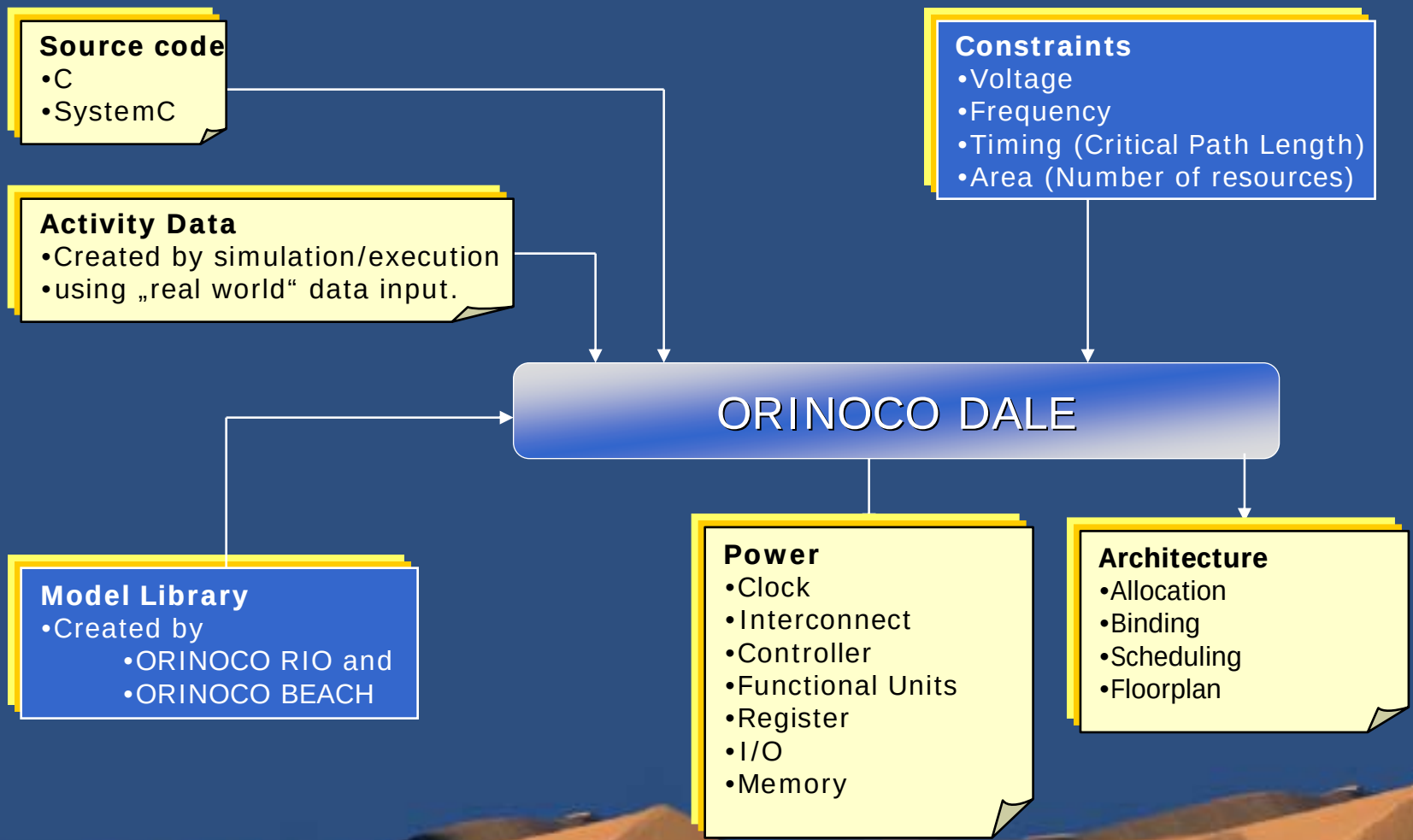
Architects and Physical Effects (1)

- It used to be possible for system-level architects to focus on the functional correctness/throughput of their designs
  - But few concerns about physical implementation issues
- The implementation teams needed to compensate for any naiveté on the part of the system architects
- As silicon technologies get more advanced, system architects need to start taking physical issues into account
  - Architectural decisions are very costly and difficult to fix at lower levels
  - Architects may not even be available to fix problems once implementation begins
    - May be working on next project

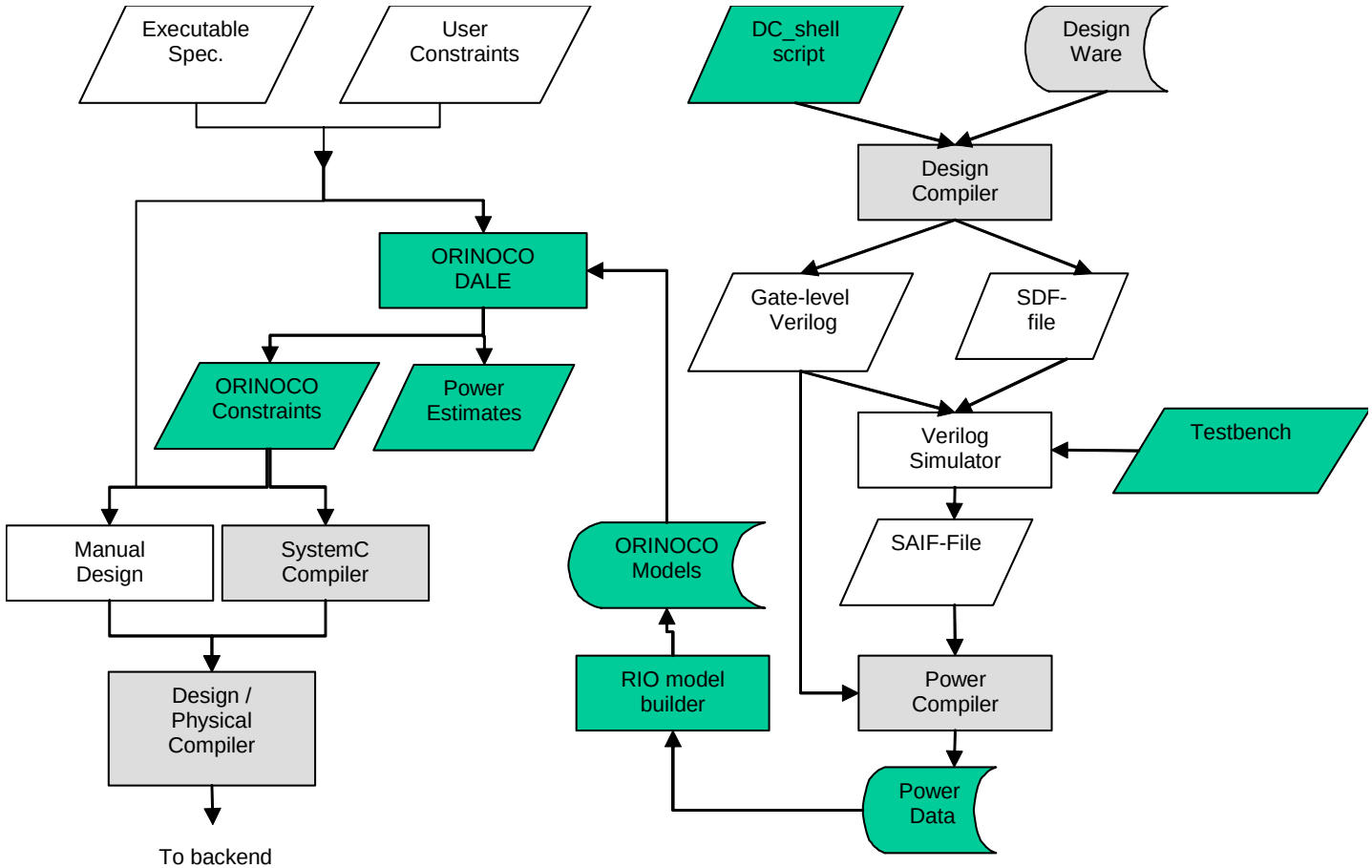
Architects and Physical Effects (2)

- System architects often do not have detailed understanding of physical effects
  - Many lack implementation experience
- Those with more implementation experience often rely on ad hoc methods like using Excel to develop power models
  - Multi-dimensional spreadsheets are now being used on many architectural teams
    - Not a sustainable methodology
- Therefore, the need arises for tools that will provide physical information:
  - In a “architect-friendly” way
  - With sufficient accuracy to guide decisions

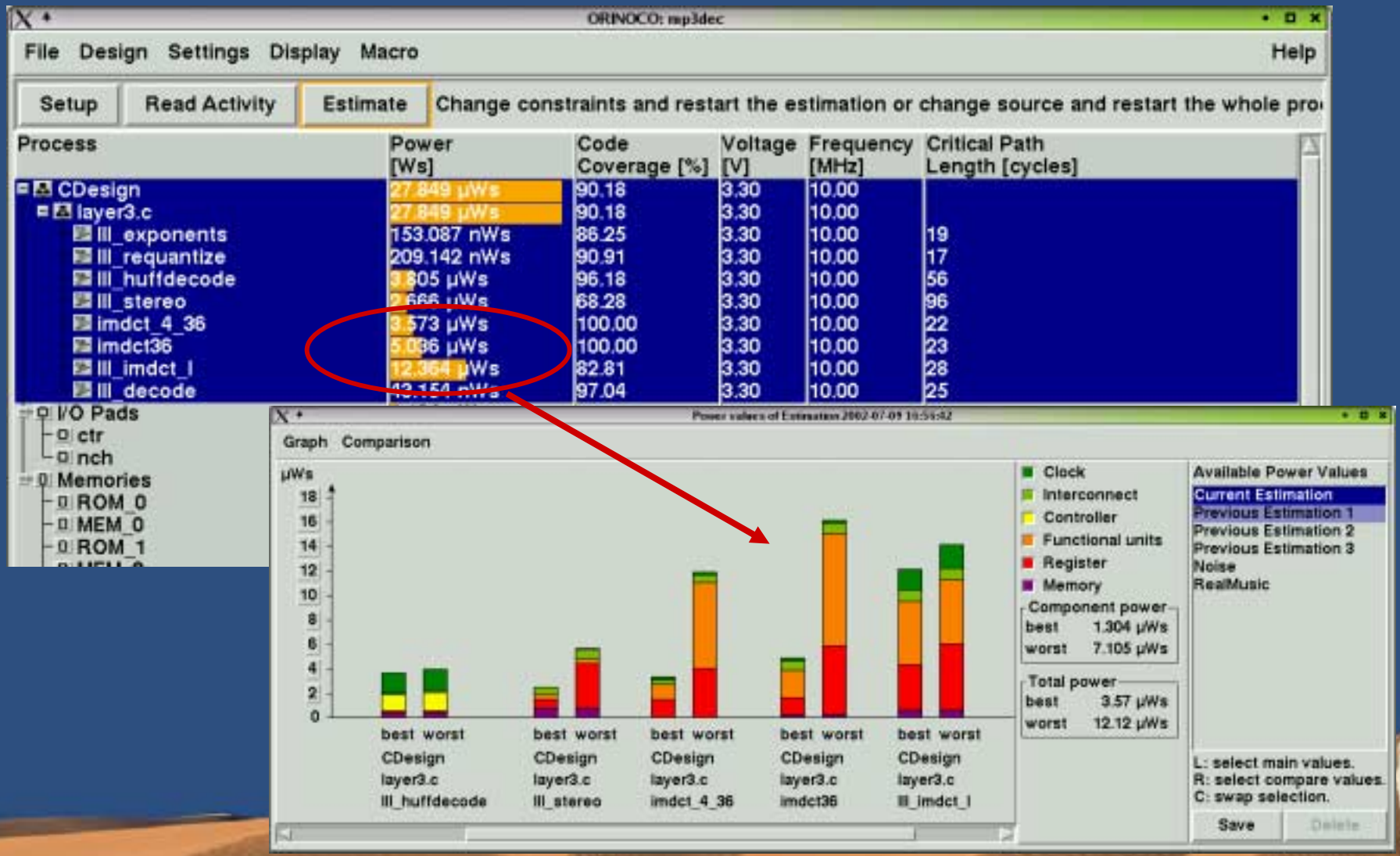
ORINOCO DALE Tool Flow



Creating a Model Library

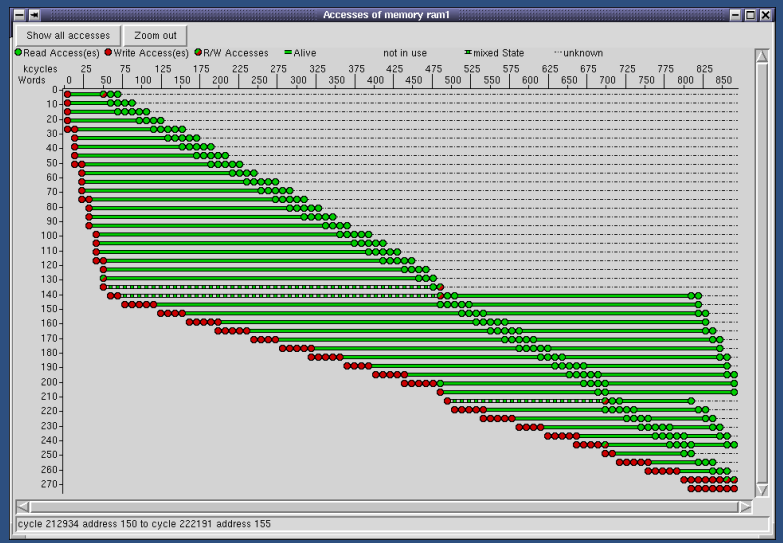


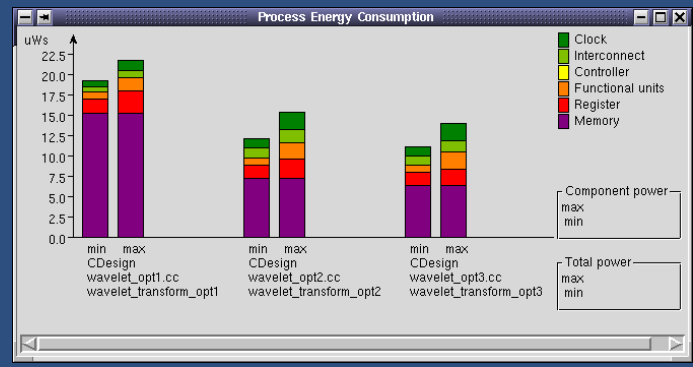
ORINOCO Power Analysis



Memory Mapping

Wavelet Transform (1D)

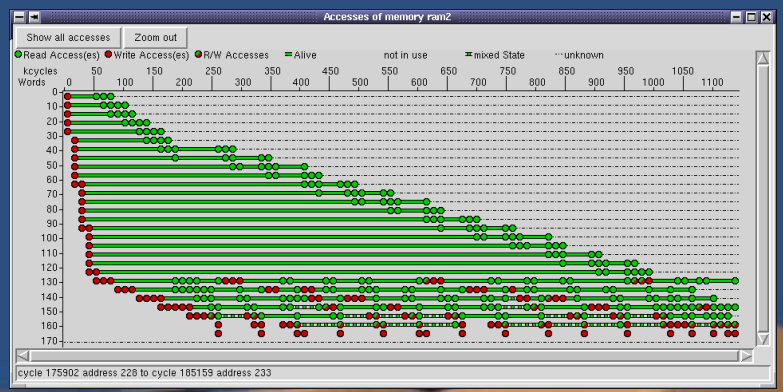


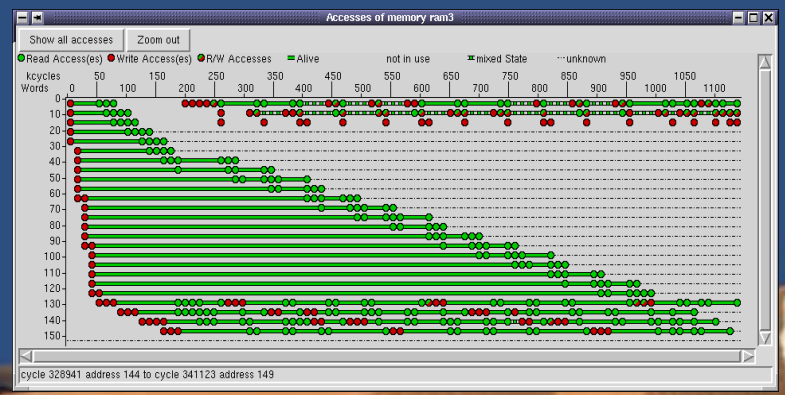


19.2 12.1 10.9 µWs

intra array optimization

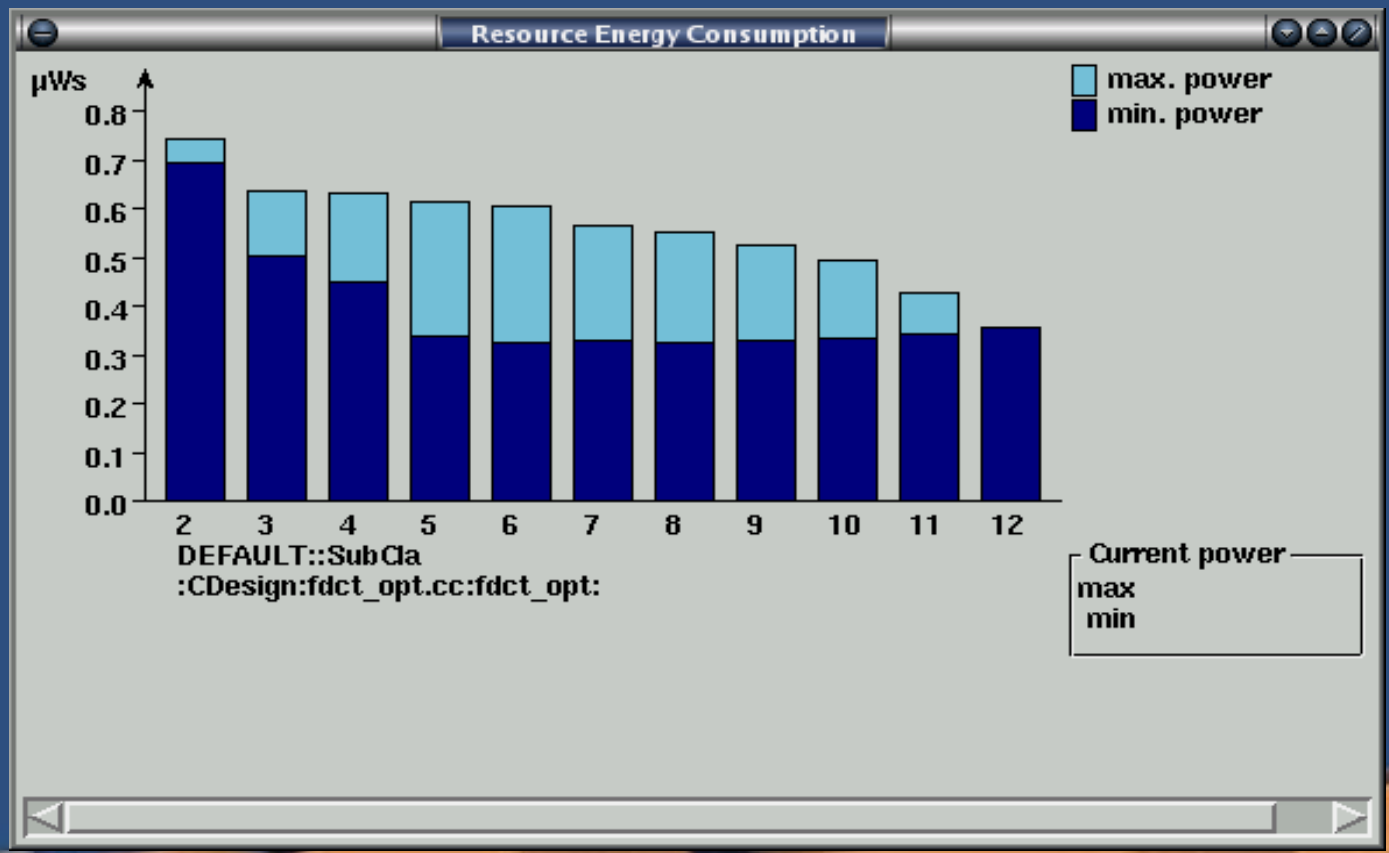
inter array optimization



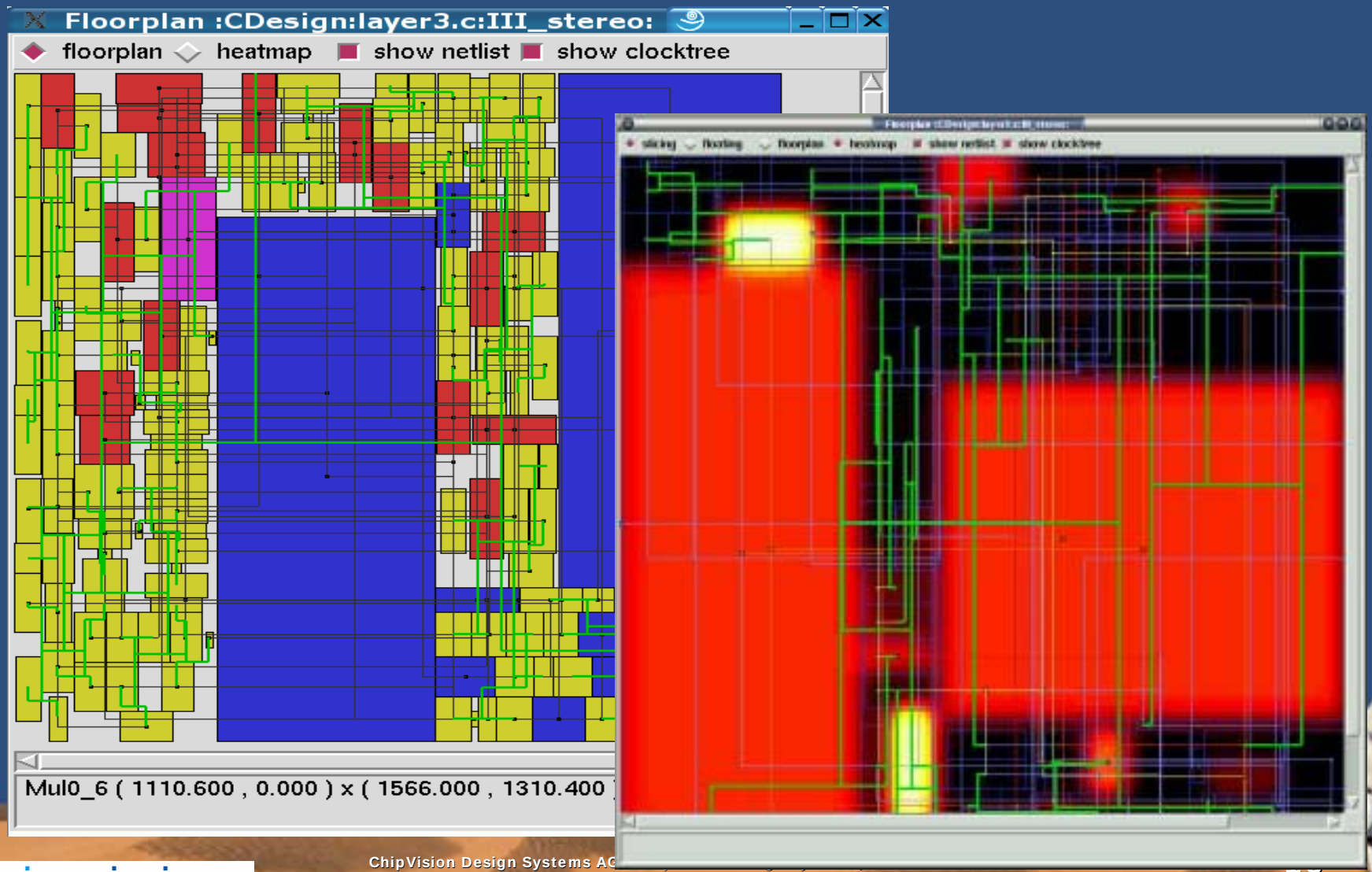


Resource Sharing / Allocation

- How many resources should I spend in my design?



Floorplannig



Current Accuracy Benchmark (Layout) Results

Resource	Count	Under-estimation	Over-estimation	Average
Adders	13	-47%	20%	-23%
Subtractors	13	-58 to -6%	-	-38%
Multipliers	16	-	23-89%	38%
Registers	44	-5%	4%	<1%
Total	-	-	-	5%