

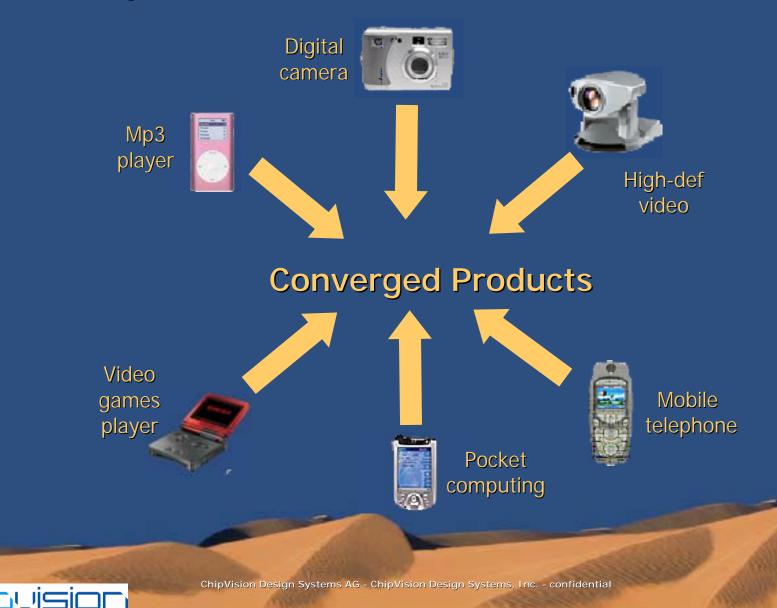
ChipVision Design Systems

Stan Krolikoski CEO

Multiple Demands on Today's IC Designers Low Power © High Density 0 00 **High Performance** 0 It's Not Just About Size and Speed Any More!



Battery Life Becomes An Issue At 135nm



At 90nm Power Is An Issue Everywhere



Data Processing



Data Storage



Military/ Aerospace



Industrial Electronics



Automotive



Consumer Electronics



Wireless Communications



Wired Communications



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EDA Has Focused on Low-Level Power Analysis



ChipVision, PowerEscape, ASC - PowerEscape complementary to ORINOCO - ASC seems to only have research tool



Sequence, Synopsys, Cadence, Atrenta, Veritools

Gate/Xstr-Level

Synopsys, Cadence, Magma, Mentor, ... - The bulk of EDA Power Tools



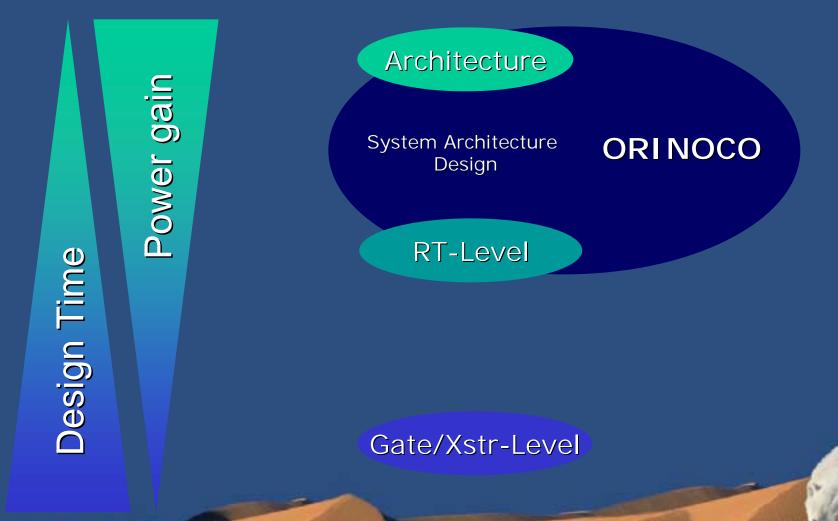
But The System Level Must Be Addressed

"For Continued Improvement in Designer Productivity, an emerging system-level of design, well above RTL, is required"

> International Technology Roadmap for Semiconductors, 2003 Edition-- Design, p. 9

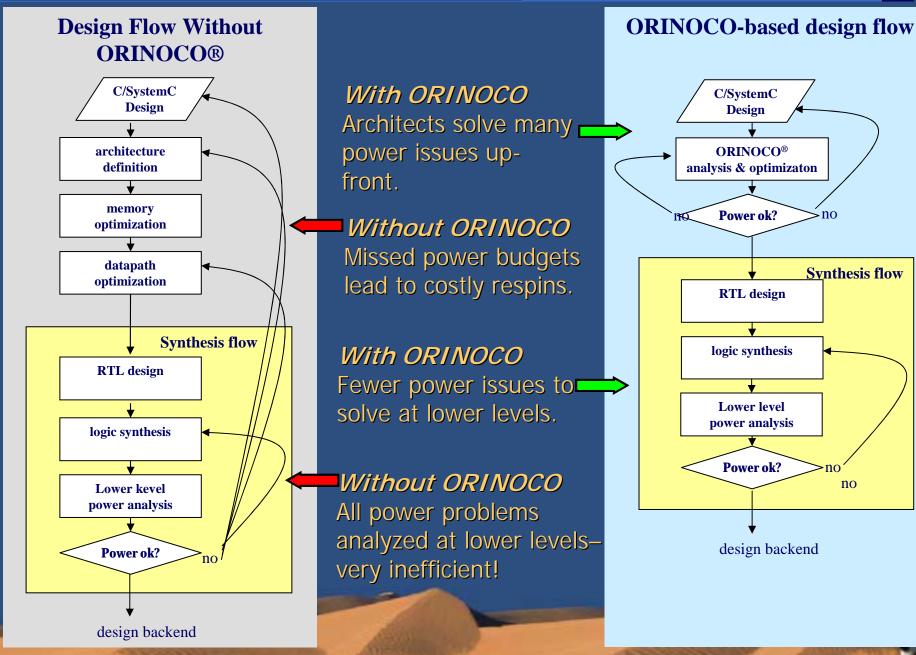


Attacking Power at The System Level



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Architects and Physical Effects (1)

- It used to be possible for system-level architects to focus on the functional correctness/throughput of their designs
 But few concerns about physical implementation issues
- The implementation teams needed to compensate for any naiveté on the part of the system architects
- As silicon technologies get more advanced, system architects need to start taking physical issues into account
 - Architectural decisions are very costly and difficult to fix at lower levels
 - Architects may not even be available to fix problems once implementation begins
 - May be working on next project

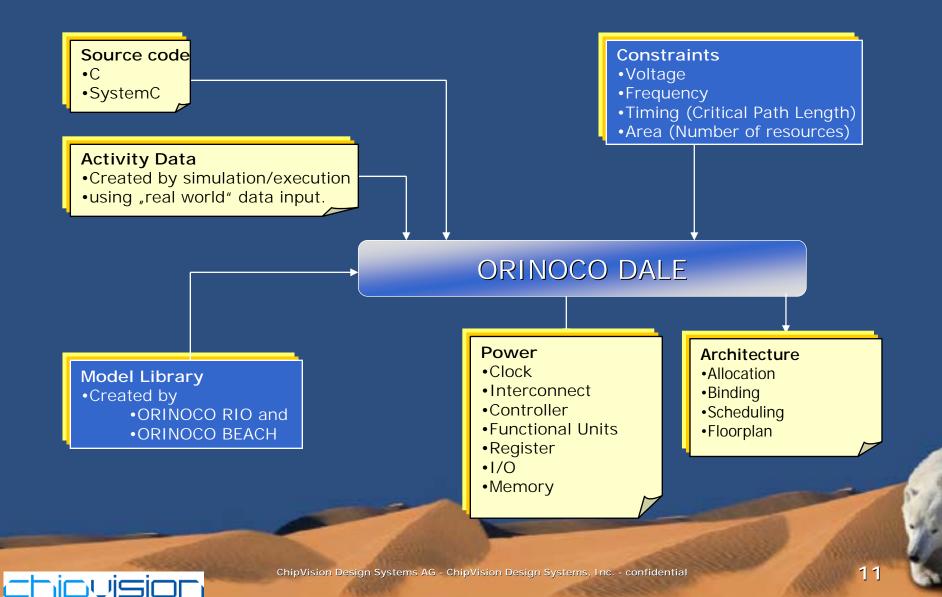


Architects and Physical Effects (2)

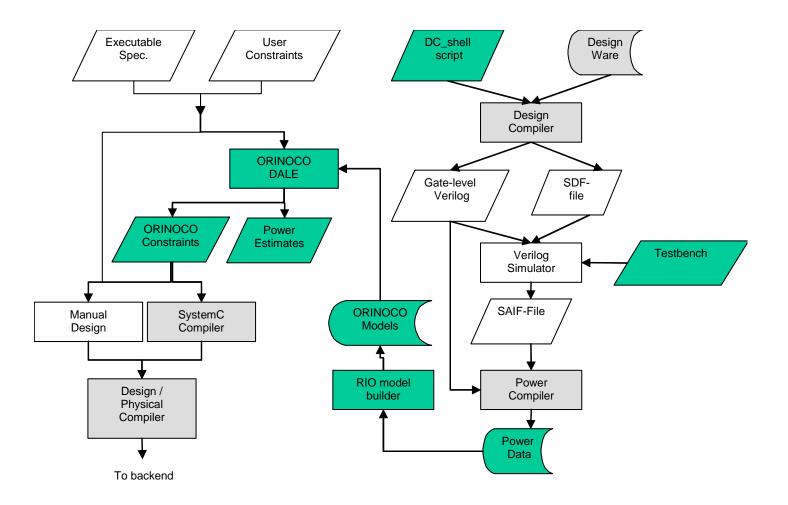
- System architects often do not have detailed understanding of physical effects
 - -Many lack implementation experience
- Those with more implementation experience often rely on ad hoc methods like using Excel to develop power models
 - Multi-dimensional spreadsheets are now being used on many architectural teams
 - Not a sustainable methodology
- Therefore, the need arises for tools that will provide physical information:
 - -In a "architect-friendly" way
 - -With sufficient accuracy to guide decisions



ORINOCO DALE Tool Flow



Creating a Model Library



ORINOCO Power Analysis

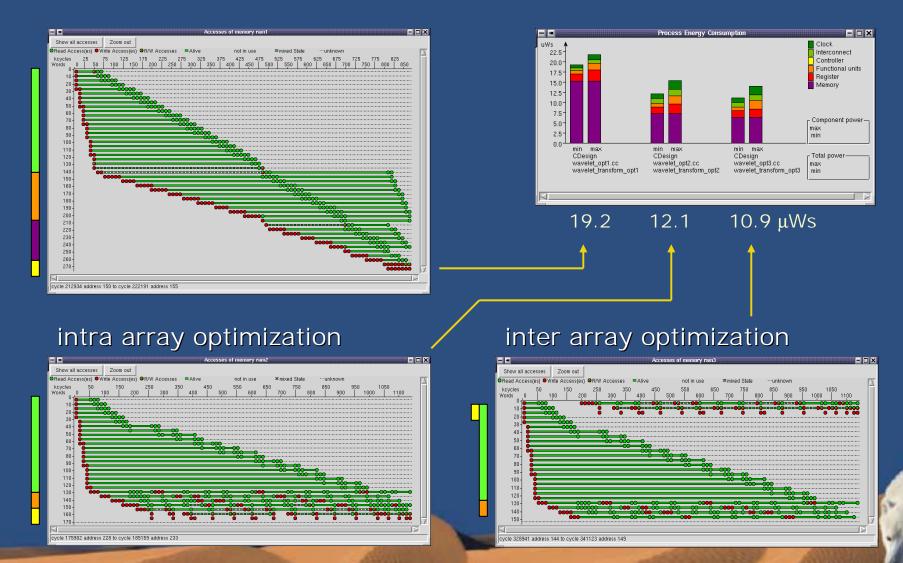
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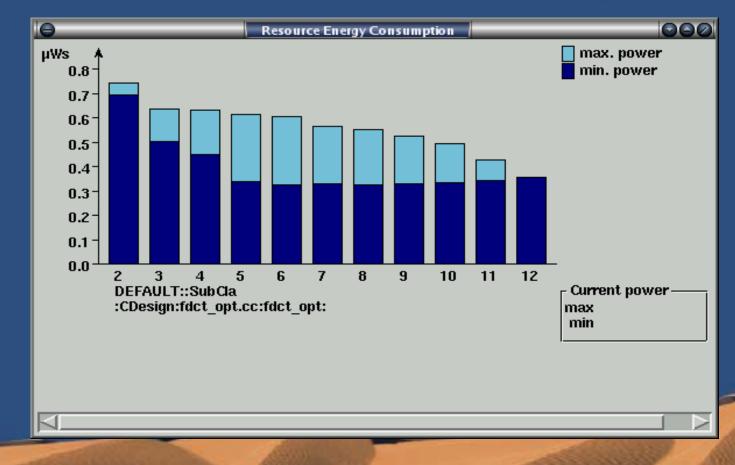
Memory Mapping Wavelet Transform (1D)



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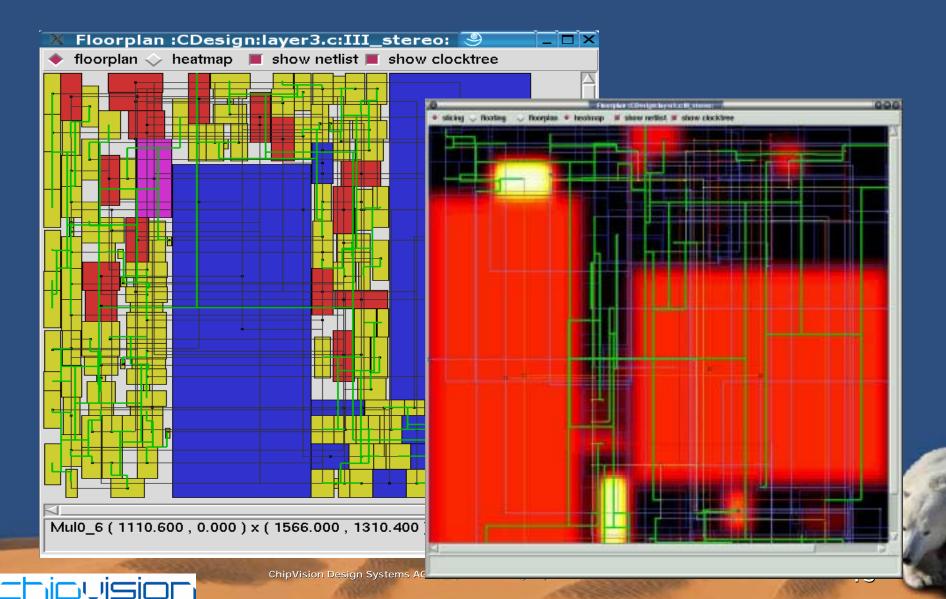
Resource Sharing / Allocation

How many resources should I spend in my design?





Floorplannig



Current Accuracy Benchmark (Layout) Results

Resource	Count	Under- estimation	Over- estimation	Average
Adders	13	-47%	20%	-23%
Subtractors	13	-58 to -6%	-	-38%
Multipliers	16	-	23-89%	38%
Registers	44	-5%	4%	<1%
Total	-	-	-	5%

