Total Hot Spot Management from Design Rule Definition to Silicon Fabrication

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Abstract

The total flow consisting of manufacturability checks (MCs) was proposed to obtain stable pattern formation without any hot spots under low-k_1 lithography condition. The MC in the lithography design stage finds out the hot spots in the model patterns created by a compaction tool, and helps to define complex design rule. The MC in design stage is important to refine the design rule and improve PPC using the actual layout patterns. Even after placement and routing, there are some risks of remaining hot spots due to topology change at the cell boundaries. It is considerably necessary to feed forward the hot spots to the mask process and wafer process. Total hot spot management from design rule definition to silicon fabrication enables to clean up the "hot spots".

1 Introduction

The shrinkage of large-scale integrated circuits (LSI) has kept around 75 % per 1.5 years constantly. However, pattern formation technologies recently don't catch up with the requirement due to their technical difficulties. Needless to say, an optical lithography is a core technology in them, which resolution is determined by the exposure wavelength, λ, and numerical aperture of the exposure tool, NA. The normalized minimum line width of the LSI, k_1, is written by

$$k_1 = L/(\lambda/NA),$$

where L is the minimum line width of the LSI. The k_1 is decreasing year by year. The low-k_1 lithography gives large optical proximity effect resulting in remarkable corner rounding, line end shortening, and critical dimension (CD) variation through pitch, etc. Besides, the loading effects not only on the optical matter but also on other pattern formation processes, naming generically a process proximity effect (PPE), are not negligible with decreasing in the feature sizes. Accordingly, a process proximity correction (PPC) technology is indispensable to obtain sufficient CD accuracy and pattern fidelity the designers need. However, the PPC technology does not always give solution for any patterns they draw unfortunately. The issue is that it is considerably difficult to make a perfect design rule for any pattern topology to satisfy condition for the solution by the PPC. This is due to the complexity of PPE resulting from all physical effects from mask making to silicon fabrication. There are some risks of "hot spots", which means a critical point having a critical process window for manufacturing, if the designers draw layouts following the imperfect design rule.

In this report, a new methodology from design rule definition to silicon fabrication in low-k_1 lithography condition was presented to manage the hot spots totally. Especially, design rule definition and manufacturability check (MC) in design stage are key technologies in the method.

2 Design rule crisis in low-k_1 lithography

Figure 1 shows available optical lithography technologies as a function of minimum line width. The normalized line width, k_1, is also shown in the figure. Optical lithography has been making great effort to catch up with the requirements for resolution, resulting from severe shrink of CDs of LSI circuits, by shortening the exposure wavelength as well as enlarging NA of exposure tools; nevertheless, k_1 factor is decreasing as the pattern size is shrinking. Figure 2 shows the impact of low-k_1 on pattern fidelity. The pattern fidelity is decreasing as decreasing in

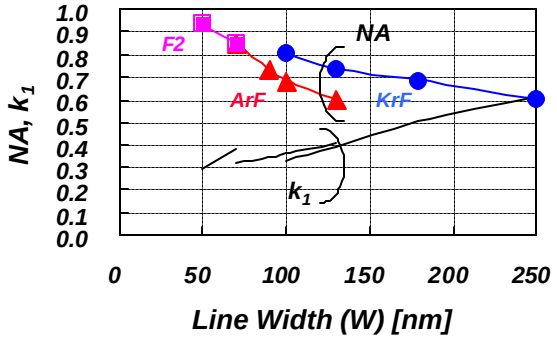

Fig. 1 Available optical lithography technologies as a function of minimum line width

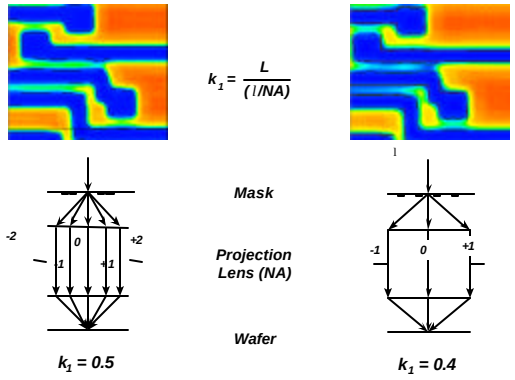

Fig. 2 Impact of low-k_1 on pattern fidelity

k_1. It is found that there is a hot spot even if the layout is drawn without violating a minimum spacing rule, and is corrected by a perfect PPC. The issue is that the positions and degrees of the hot spots don't depend only on the space width and/or neighboring line width. A simple minimum spacing and line rule can't clean up the hot spots at all. Optical lithography simulation tells us the positions of the hot spots, but it is critical to define the adequate rule for the dangerous topology; not too aggressive, not too moderate.

3 Strategy and the total development flow for DfM

What total development flow from design rule definition to silicon fabrication should be under the condition? Figure 3 represents the schematic illustration of the strategy for design for manufacturability (DfM). The horizontal axis shows the k_1 factor, and the vertical axis is the complexity of the design rule. Conventionally, the design rule was simple, e.g. minimum line width, minimum spacing, etc., due to the small PPE in the large k_1 factor world, around 0.5. In low-k_1 lithography, the simple design rule can't guarantee the resolution of all kind of pattern variations due to its large PPE. There are two main approaches for solving the issue. One is the complex design rule approach, and another is the simulation based MC approach. MC compares a target layout and a simulated image of the PPCed mask data, and highlights portions of greater difference than a criterion between the two as hot spots. The former approach yields few hot spots due to the complex design rule, but it takes long time to define the design rule. Besides, the complex design rule makes designers feel hard to draw layout. On the contrary, the latter approach yields relatively many hot spots due to the simple design rule, and makes the designers waste time and labor to repair the hot spot, but it takes short time to define the design rule. The realistic approach should be the combination of the two approaches described above. First of all, lithographers should define as accurate design rule as they can, using as many pattern variations as they can; not only simple patterns but also pseudo-real device patterns at the stage of design rule definition. Secondary, the design rule should be refined by the MC in the design stage using the actual device patterns. For memory device case, there is an advantage of the MC because it is important for memory device to reduce cost by shrinking the chip size.

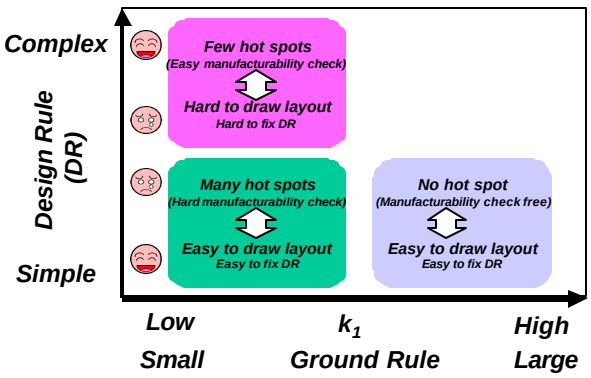

Fig. 3 Schematic illustration of the strategy for design for manufacturability (DfM)

Figure 4 shows the total development flow for DfM based on the concept described above. First of all, device engineers and designers show lithographers CD tolerance

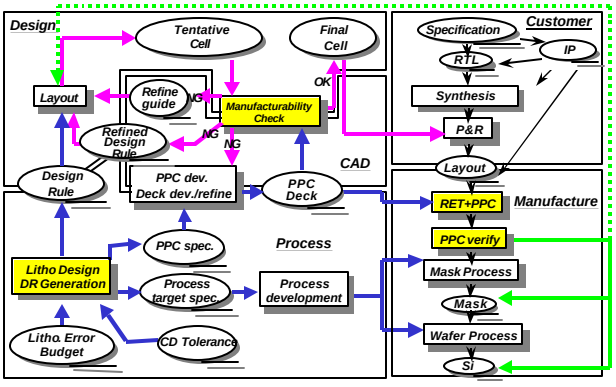

Fig. 4 Total development flow for DfM

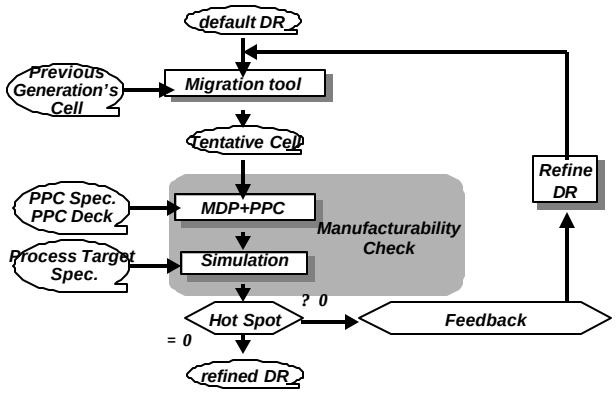

Fig. 5 Flow of design rule definition

for next generation's device. In order to obtain sufficient CD accuracy, the process engineers, especially lithographers carry out the simulation and experiment to determine the lithography method and conditions having sufficient CD accuracy less than the estimated CD tolerance. They define the drawing regulation, forbidden rule to obtain sufficient accuracy of pattern formation under the estimated lithography method and conditions. At the same time, they require target specifications for all kinds of process technologies, e.g. resist and etching performance, PPC method and algorithm, RET technologies, and so on. We call this procedure "lithography design." The designers start to layout according to the agreed design rule. The balance between the design rule and the target process technologies are considerably significant. If the target process technologies are too severe and the resultant design rule is too aggressive for the next generation's device fabrication, it is hard to make. On the contrary, the chip is not highly competitive if the target process technologies are not severe and the resultant design rule is too moderate. In this timeframe, there is no actual layout. We use previous generation's layout as the model patterns of the next generation to achieve accurate design rule. The detailed flow is described later.

MC for the tentative cells following the design rule is carried out in the design stage. The MC flow consists of PPC and simulation for pattern formulation including lithography. There are three feedback passes in case there are some hot spots in the cells. One is to improve PPC deck and PPC parameters, another is to repair the hot spots, and the other is to refine the design rule itself. The sort of device, timing, and so on dominates which pass is a main stream.

Place and route system uses the complete cells to build full-chip physical layout. Design rule checker (DRC) finds out the design rule violation and MC finds out the hot spots in the full chip layout data. MC compares a target layout and a simulated image of the PPCed mask data, and highlights portions of greater difference than the criterion between the two as hot spots. There is an opportunity to occur the hot spots even in this stage. In this case, there are few chances to feed back the hot spots to the design procedure. Therefore, it is considerably necessary to feed forward the hot spots to the mask process and wafer process. A metrology tool to navigate any hot spots portion and to measure the pattern quickly is essential for the flow in low-k_1 lithography world.

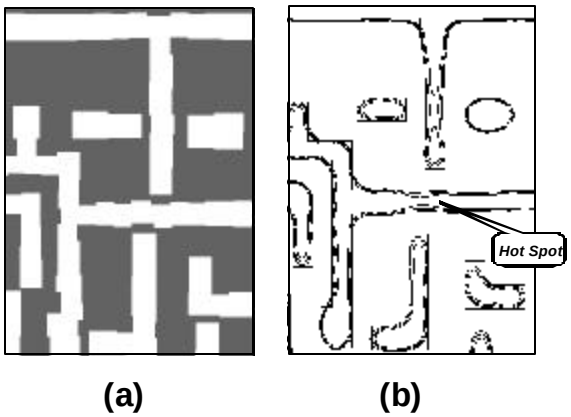

Fig. 6 (a) PPCed mask patterns for the shrunk patterns from 130-nm node to 65-nm node following tentative design rule for 65-nm technology node , (b) the simulation result for the PPCed mask patterns overlaid by the target patterns

4 Lithography design and design rule definition

Figure 5 shows the flow of design rule definition. In this timeframe, there is no actual layout. We use previous generation's layout as the model patterns of the next generation to define accurate design rule. After determining lithography method, condition, and tentative design rule with simple representative patterns, the previous generation's primitive and/or macro cell patterns are shrunk by any compaction tools, e.g. migration tool, following the tentative design rule. The shrunk patterns are converted into PPCed mask patterns. The PPCed mask patterns are transferred by simulation for pattern formulation including lithography, and compared with the target patterns to find the hot spots. If there are some hot spots, the design rule is refined to eliminate the hot spots. The iteration of the procedure makes the design rule eliminate the hot spots. Figure 6 shows the example of the procedure. Figure 6(a) shows PPCed mask patterns for the shrunk patterns from 130-nm node to 65-nm node following tentative design rule for 65-nm technology node. Figure 6(b) shows the simulation result for the PPCed mask patterns overlaid by the target patterns.

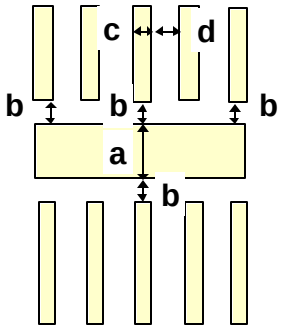

Fig. 7 Simplified and modeled patterns of the layout shown in Fig. 6 to obtain critical CD of line width "a"

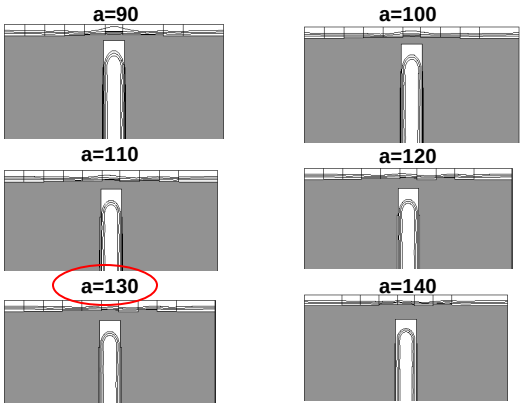

Fig. 8 Simulation results of the feature "a" for b = 1000 nm

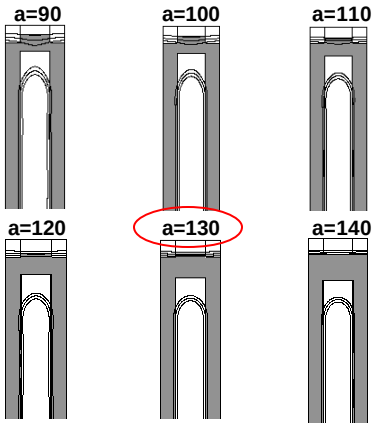

Fig. 9 Simulation results of the feature "a" for b = 90 nm

There is a hot spot for line narrowing at the portion nipped by two bars. The pattern fidelity at the hot spot is getting worse than the other portion with increasing in dose error. Next, it is necessary to find the adequate line width not to be line narrowing even with dose error. The hot spots patterns are simplified and modeled as shown in Fig. 7, and the adequate design rule is obtained by the parametric running of the patterning simulation. Figures 8 and 9 show the results. It is found that the line width of the design layout, a, should be more than 130 nm to maintain the corresponding line width on the wafer. The design rule has grown to cover as many pattern variations as the lithographers can in the lithography design stage according to the procedure.

5 Manufacturability check

Figure 10 shows the detailed procedure for MC in design stage. The designers draw the tentative layout following the design rule defined by the lithography design process. The patterns are converted into PPCed patterns, and the PPCed mask data are checked by simulation based verification tool to find the hot spots. There are three-feedback pass in case there are some hot spots in the cells. One is to improve PPC deck and PPC parameters, another is to repair the hot spots, and the other is to refine design rule itself. The improvement of PPC deck and PPC parameters to eliminate the hot spots should be prioritized rather than the other feedback passes. However, it is impossible to say definitely that there is no probability to feed back to the repair of the hot spots and/or the refinement of the design rule in the development stage. Figure 11 shows an example that changing the PPC parameter on the minimum jog length can eliminate the hot spot. The upper figures show the PPCed patterns of gate level of SRAM cell for 90-nm technology node overlaid with the active patterns, and the bottom ones are the corresponding simulated images on the wafer printed by ArF exposure tools. The longer jog length was not enough to control local CD variation at the curved

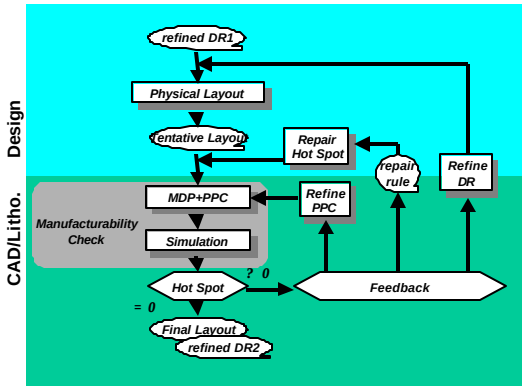

Fig. 10 Detailed procedure for MC in design stage

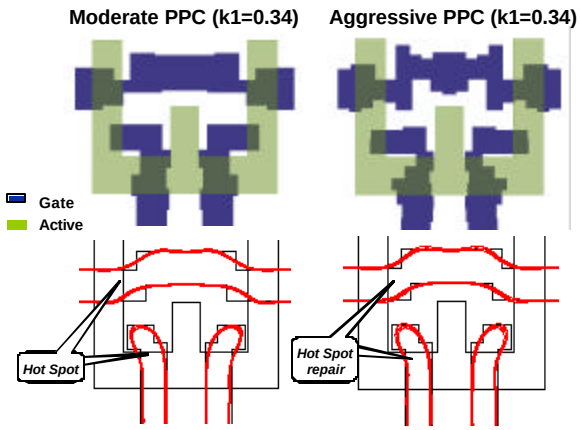

Fig. 11 Hot spot elimination by shortening jog length

portion of the gate patterns. The shorter jog length improved the local CD controllability. However, the shorter jog makes the reticle writing time elongate for a variable shaped beam type electron beam writer. It also makes other issues for reticle manufacturing. Shortening the minimum jog length is relatively easy way to avoid the conflict between design layout and PPCed mask layout. However, it should be determined very carefully by total optimization for efficiency and manufacturability. The MC procedure during the development stage makes the design rule robust. For volume production stage, there will be a rare case for hot spot repair or design rule refinement due to the robust design rule.

6 Hot spot management on reticle and wafer

Even after placement and routing process, there are some risks of remaining hot spots. This is because cell placement changes the pattern topology at cell boundaries against the individual cell. The change of pattern topology results in the change of PPE. In this timeframe, there are few chances to feed back the hot spots to the design procedure. Therefore, it is considerably necessary to feed forward the hot spots to the mask process and wafer process [1][2]. The feed forward pass should be a way of emergency evacuation for rare case of unavoidable hot spots. The accurate and robust design rule defining procedure being consistent with the manufacturability is extremely important for the low-k_1 lithography.

Figure 12 shows top-down scanning electron micrographs of hot spots pattern searched by the navigation system with the hot spot map on the CAD layout. The CAD layout is overlaid with the micrographs. The system makes it possible to run the production lots under the ultra-narrow lithography window condition.

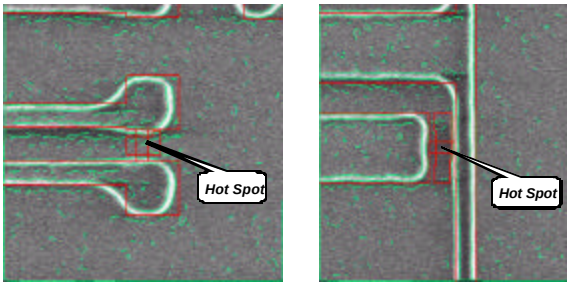

Fig. 12 top-down scanning electron micrographs of hot spots pattern searched by the navigation system with the hot spot map on the CAD layout. The CAD layout is overlaid with the micrographs

7 Concept of tolerance based PPC

To begin with, what are the criteria of the hot spot? The designers and device engineers usually give the lithographers the allowable CD error of +/- 10% of the main feature sizes. Is it really necessary for any pattern edge of any level to position within +/- 10 % of the target position? The device does work well even if the part of achieved edge positions are out of the tolerance. This is the reason why there are too many pseudo-hot spots, that is noises, which does not affect on the real device performance. Figure 13 shows the schematic illustration of LSI design with the tolerance of each pattern edge being analogous to the mechanical design form. The accurate tolerance of each edge position is quite necessary to eliminate the noises for MC [3][4].

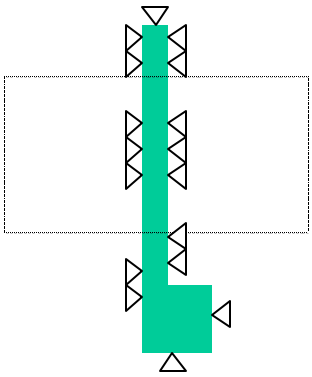

Fig. 13 Schematic illustration of LSI design with the tolerance of each pattern edge being analogous to the mechanical design form

8 Summary

The total development flow consisting of three MCs was proposed to obtain stable pattern formation under low-k_1 lithography condition. It is hard to define accurate and robust design rule under the condition because there are large and complicate PPE. Of course, there is no actual process and layout in the design rule defining stage. The compaction tool helps to make model patterns of the next generation. MC finds out the hot spots in the model patterns, and helps to define complex design rule. However, the design rule might be imperfect due to large PPE. MC in design stage is important to refine the design rule and improve PPC flow using the actual layout patterns. It is essential for the designers not to have a heavy load. Even after placement and routing, there are some risks of remaining hot spots due to topology change at the cell boundaries. In this timeframe, there are few chances to feed back the hot spots to the design procedure. Therefore, it is considerably necessary to feed forward the hot spots to the mask process and wafer process. Total hot spot management from design rule definition to silicon fabrication makes it possible to obtain higher yield for 65 nm and beyond generations.

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