The importance of layout density control in semiconductor manufacturing

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Abstract

This paper shows that specification of simple constraints on layout density can result in substantial reduction of within-die variation in a number of different processes. The concept is illustrated with examples of characterization of process-layout interaction based on layout density, and subsequent control of process variation through control of this density.

1 Introduction

As the demand for high performance IC products continues to grow, the industry has sought to reduce both device size and within-die variation of these devices. To achieve this, process development engineers have needed to address both these aspects in delivering processes to the factory, often having to balance opposing directions. For example, in lithography development, a higher numerical aperture of the stepper lens is necessary for printing smaller poly lines, but this also reduces the depth of focus needed for process robustness. While creative process engineers and materials scientists have managed to juggle such varied requirements to eventually deliver a process that meets them all, this has ended up pushing processes to a point where the slightest variation in operating conditions can cause instability and, often, fatal loss of yield.

Designers and process engineers have tried to address this present and deepening crisis with a number of collaborative approaches (Reference 1). One approach has been to accept intrinsic limitations in individual process modules, and compensating for them by tuning other modules, as well as the design itself. This has suggested the coupling of TCAD and ECAD tools – an approach that is promising but not without pitfalls. The two main problems with the concept of using coupled tools and methodologies are 1) a significant increase in design time, and 2) greater probability of small errors multiplying without early detection. These reasons have so far limited widespread proliferation of coupled tools, although this will change when the related economics become favorable. The other approach designers and process engineers have used is to agree on additional design rules, intended to make the processing easier, or even feasible in some cases. These design rules vary in terms of complexity of specification and the extent of restrictions they require. The most frequent and restrictive proposals (as evident, say, from the body of recent literature on design-process integration) arise from a lithographic perspective, which is not surprising if one considers the relative cost of patterning, particularly going from one generation to the next. An example of one of the more radical design rule proposals is designing on a regular, coarser grid, which would allow the lithographer to focus the process to print primarily lines and spaces, which in turn can be improved by several techniques such as the use of Alternating Phase Shift Masks. Needless to say, such dramatic proposals pose greater challenges to the designers and as such are slower to materialize. Other design rules are less radical but still require substantial change in the design process; an example is the orientation of gates in a single direction to diminish the impact of lens aberrations that cause differences between horizontal and vertical features.

This paper addresses a simpler design rule – concerning layout density – and provides rationale and some examples from a process development perspective to highlight the importance of this aspect of design-process integration.

2 Shrinking Process Margins

It is useful to briefly review the shrinking process margins encountered by process engineers today, as a motivation for instituting any design methodology changes. In order to limit the scope of that review, this section will focus on process margins in lithography, partly because the lithography process latitude budgets often indirectly take into account the variations in other processes such as Chemical-Mechanical Polishing. In order to do this, let us first introduce here the term NILS, or Normalized Image Log Slope. This metric has been used to describe the process latitude in lithography, and can be described as the percentage change in exposure dose needed to cause a unit percentage change in patterning CD (e.g. the width of a line). By calculating NILS at various defocus conditions, lithographers obtain a measure of process latitude in both dose and defocus. Defocus, in turn, is caused by a number of effects in the process, one of them is the topography variation in the thin film over which the photoresist is spun. Figure 1

shows that NILS values have been decreasing for subsequent process technology nodes. In other words, the process margin in lithography, to accommodate process variation in other process modules, has been decreasing. Similar trends can be documented for other process modules, and it is accurate to conclude that most process modules are becoming sensitive to various process parameters.

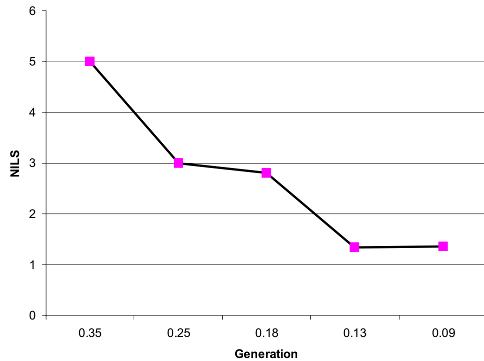

Figure 1: A plot of Normalized Image Log Slope at maximum allowed defocus versus technology node

One such process parameter for many wafer process modules is the layout pattern that has been "inscribed" in the wafer before that processing step, or, in the case of photolithography, the layout pattern in the mask for that process step. Depending on the details of the given process, different layout patterns can cause different processing end results. The central point of this paper is that, for many processes, a simple layout property, namely feature density, is increasingly useful in characterizing the nature of the process-layout interaction. Understanding this interaction is particularly useful in the face of the aforementioned shrinking process margins.

Next we will consider two examples of interaction of layout with process, and illustrate the use of layout density to characterize these interactions.

3 Addition of dummy features for CMP uniformity

The first example of process and layout interaction concerns the Chemical-Mechanical Polish (CMP) process. It has been observed that the rate of polishing is proportional to the pressure that the polishing pad exerts at the point of contact between the pad and the topographically uneven film being polished. Given a constant force on the pad, this translates to a greater pressure when a fewer number of topographic "hills" are in contact with the pad. In other words, the rate of polish is greater when the density of layout features that are patterned as hills is smaller; this is illustrated in Figure 2.

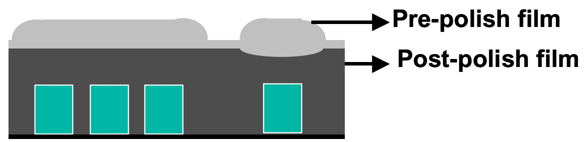

Figure 2: A schematic of the dependence of polish rate on layout dependent wafer topography.

This allows one to model CMP as a function of layout density, and subsequently calculate within-die variation of thickness of the polished film. Needless to say, microprocessor chips are not characterized by repetitive features, i.e. the layout density of these chips is not uniform. As a result, the post-polish film thickness is very non-uniform. As was noted earlier, this non-uniformity can cause local defocusing in subsequent lithography steps, which in turn results in flawed patterning due to the reduced process margins.

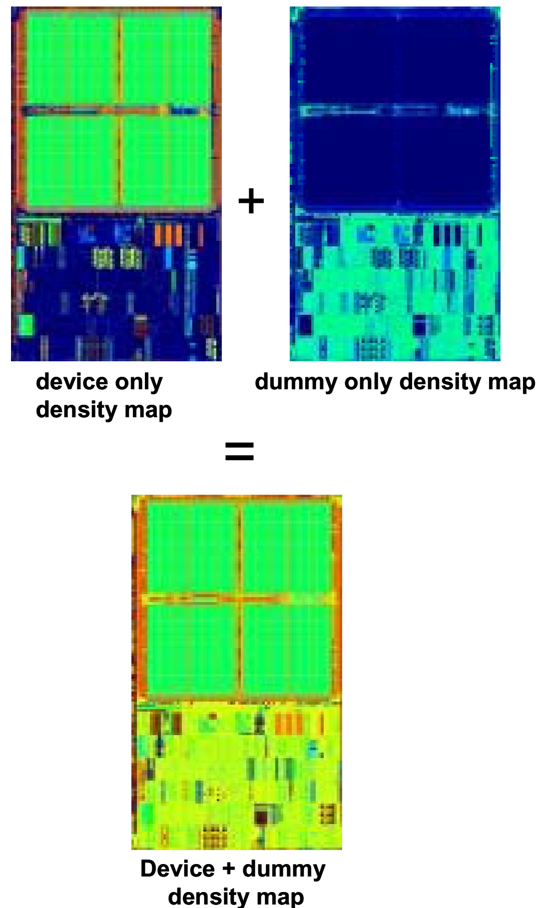

Figure 3: Thin film thickness variation before and after dummification.

One way to overcome this cascading chain of variations and failures is to minimize the variation in layout density by adding dummy features in relatively “open” areas. One illustration of the usefulness of this dummification for CMP uniformity is shown in Figure 3, which is a map of the layout density of a chip, defined as the percentage of the area in a given area (typically about
10µm X 10µm) covered by chrome. Note that the map before dummification shows a wide variation in this layout density. In order to suppress the resulting non-uniformity of the polished film, dummy features are added; a map of this dummy density is also shown. The two maps are added together to get the layout density of the final chip. If this process is iterated while varying the size of the dummies, one arrives at a final layout density map that has minimum variation.

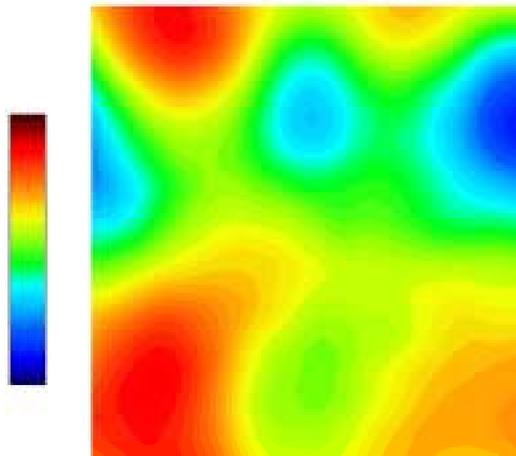

Figure 4: Modeled device performance before dummification.

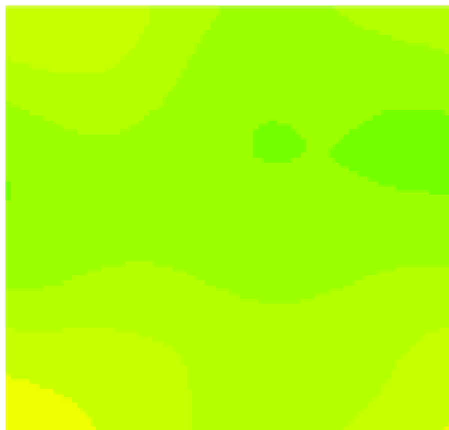

Figure 5: Modeled device performance after dummification.

Thus, the specification of a simple design rule constraining the layout density within a range is necessary to enable a relatively robust CMP process, and subsequently good lithography. The key here is to specify the “window” over which this density needs to be calculated. This window arises from the length scale characterizing the physical process – a parameter that can be obtained both from empirical characterization of this variation as well as analytical or numerical investigation of the underlying phenomena.

It is interesting to note that making the layout density more uniform can affect more than one process modules. For example, besides the variation arising during the CMP process as described before, layout density can also include the etch process. This is commonly referred to as “microloading”, alluding to a mechanism wherein etch precursors are consumed at a greater rate in areas which have a greater density of surfaces that are subject to etching. Figures 4 and 5 show a variation in modeled device performance before and after the addition of dummy features, and it is suspected that the post-dummification uniformity results from both polish and etch improvements.

While the process of dummification for improved CMP has existed for a while, new advances in this field will include the process of coupling this simulation with other modules. For example, one might use the final film thickness uniformity map as an input to a lithography simulator. Depending upon the resist planarization conditions, this integrated simulator can be used to study the CD variation across the chip as a function of film uniformity.

4 Layout dependent flare in EUV

The second example of process design interactions is taken from a process technology for the future: EUV lithography. It has been found that residual roughness on the mirrors that act as optical elements in the EUV system causes undesirable light scattering, referred to as flare. This flare has the effect of altering the critical dimension of features, by a mechanism roughly similar to introducing extra exposure dose. If the flare were constant across the entire die, the problem would be less significant; unfortunately this is not the case.

One would like to calculate the effect of mask layout on the flare at any given point on the wafer. In order to do that, it is useful to derive a point spread function, PSFsc representing the scattering by the roughness in the mirrors (References 3, 4). This PSFsc can then be convolved with the aerial image of the mask to give the resulting flare variation across the die. The following equation gives an example of such a PSFsc, which is

representative of the early EUV systems that have become available.

$$\mathrm{PSF_{SC}} = \frac{0.166}{r^{2.39}} \frac{1}{\mathrm{nm}^2} \quad \text{for } r > 600\text{nm, zero otherwise}$$

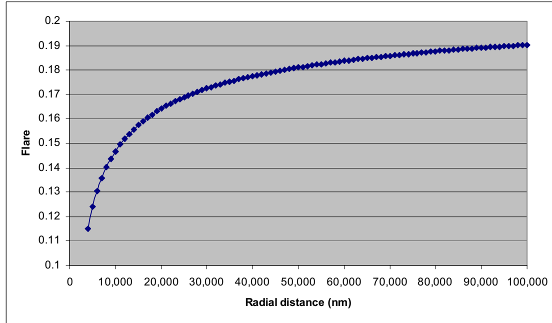

Figure 6: The cumulative contribution of flare as a function of distance from the point of calculation.

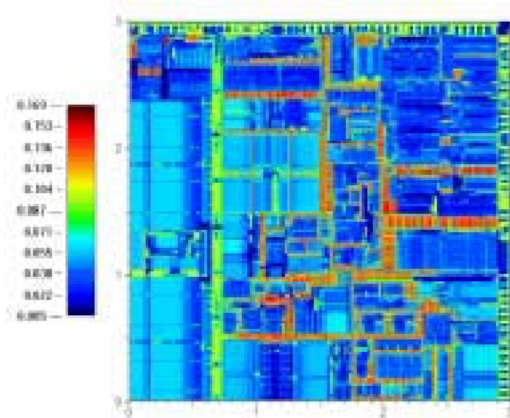

Figure 7: The variation of flare within the die.

Note that the value of this PSFsc first falls relatively quickly away from the point of interest, but then decays much more slowly. This means that the layout has a strong non-local effect on the flare at any point: even features that are millimeters away from this point affect the flare. This slow fall-off is plotted for an open frame exposure in Figure 6. To study this effect, a piece of layout from a processor of the 0.18 µm technology generation was extracted, and shrunk by a suitable factor to give an estimated piece of layout to be manufactured by EUV technology. The feature density of this layout was extracted, and convolved with the PSFsc function to give an approximation of the flare variation within this piece of the layout, as shown in Figure 7. It is clear that this flare variation will be minimized if feature density variations in the layout are minimized. This leads to either a direct constraint on the feature density variations of the layout to be imaged by EUV lithography, or the concept of placement of dummy features in the layout to indirectly constrain feature density on the appropriate grid. The dummification schemes will probably need some modification for application to EUV lithography. It is to be noted that one special consideration would be the fact that the edge of the field would normally receive less flare than the center of the field. Two possible methods of addressing this concern are listed here. The first would involve an investigation of whether the optical system can be modified, without other deleterious effects, in a manner such that the lower flare at the edge of one die is compensated by additional flare during the exposure of the adjacent die. The second possible solution is to vary the size of the dummies as a function of location within the field. Clearly, the exact scheme for EUV dummification requires further study.

5 Discussion

In the preceding two sections, we have seen that controlling layout density has great potential to improve the subsequent manufacturing, particularly for reducing within-die variation. Given that process capability of any module in today's environment has a component relating to within-die variation, it follows that this capability can be improved at least to some extent by specifying design rules on layout density, while not having to resort to more expensive or exotic processing techniques. The key reason for the increasingly urgent discussion on design process integration is that economics prohibits process engineers from delivering process capability for unrestricted layout – clearly layout density control is one of the simpler restrictions.

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