Designing-in Test & Repair IP for Manufacturing Yield

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Contents

- Deep Submicron Trends
- SoC yield & reliability challenges
- Optimization loop concept
- Infrastructure IP & resource partitioning
- Examples in embedding infrastructure IP
- Conclusions

Deep Submicron Trends

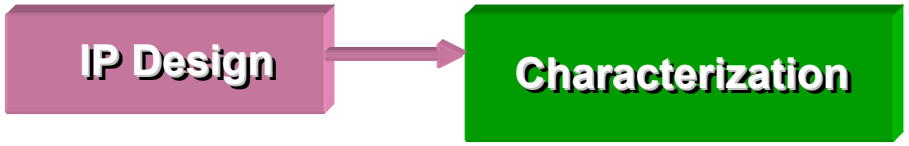
- Number of transistors
- Mixed technologies
- Shriking geometries
- Process layers
- New process material
- High performance

Deep Submicron Impact

- Miniaturization and High Performance result in
  - Finer and denser semiconductor fabrication
  - Increased susceptiblity
  - Increased defectivity
  - Lower manufacturing yield and reliability
- Observed as
  - Defect density
  - Realistic Faults
  - Timing problems
  - Transient or Soft Errors

IC Realization Flow

IC Realization Flow



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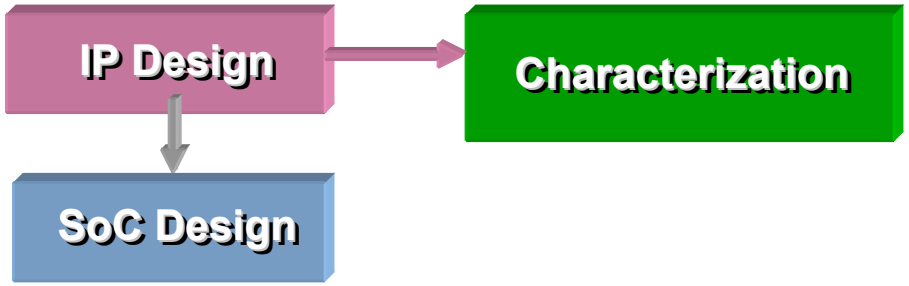

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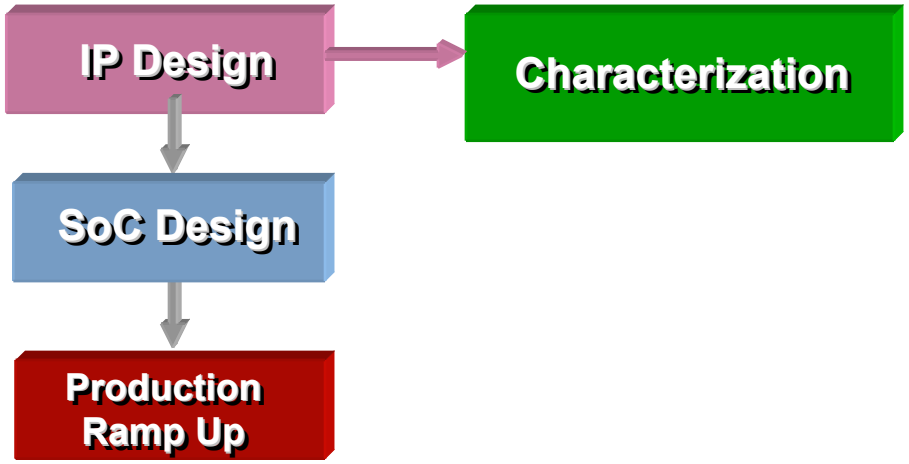

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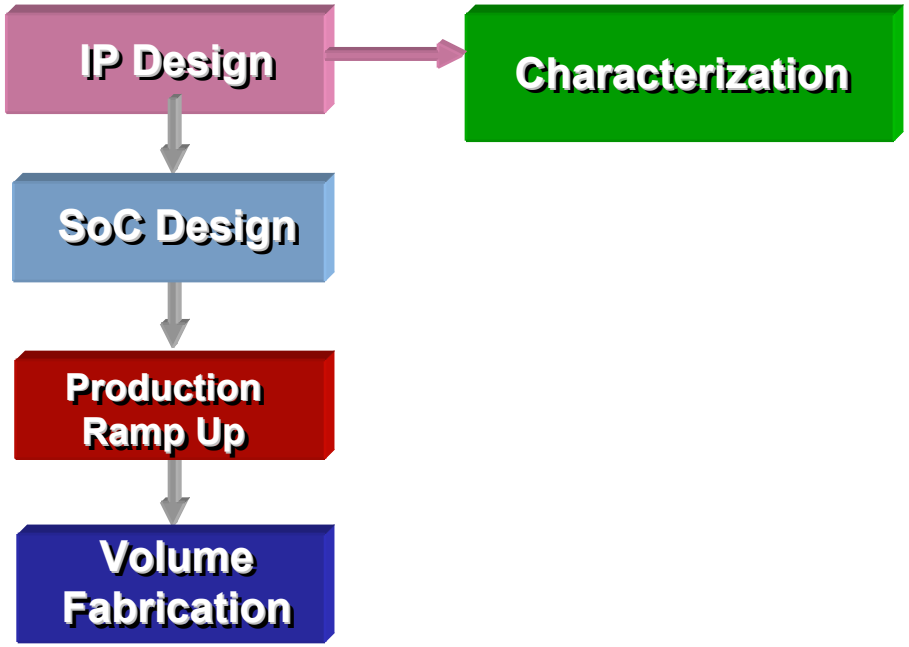

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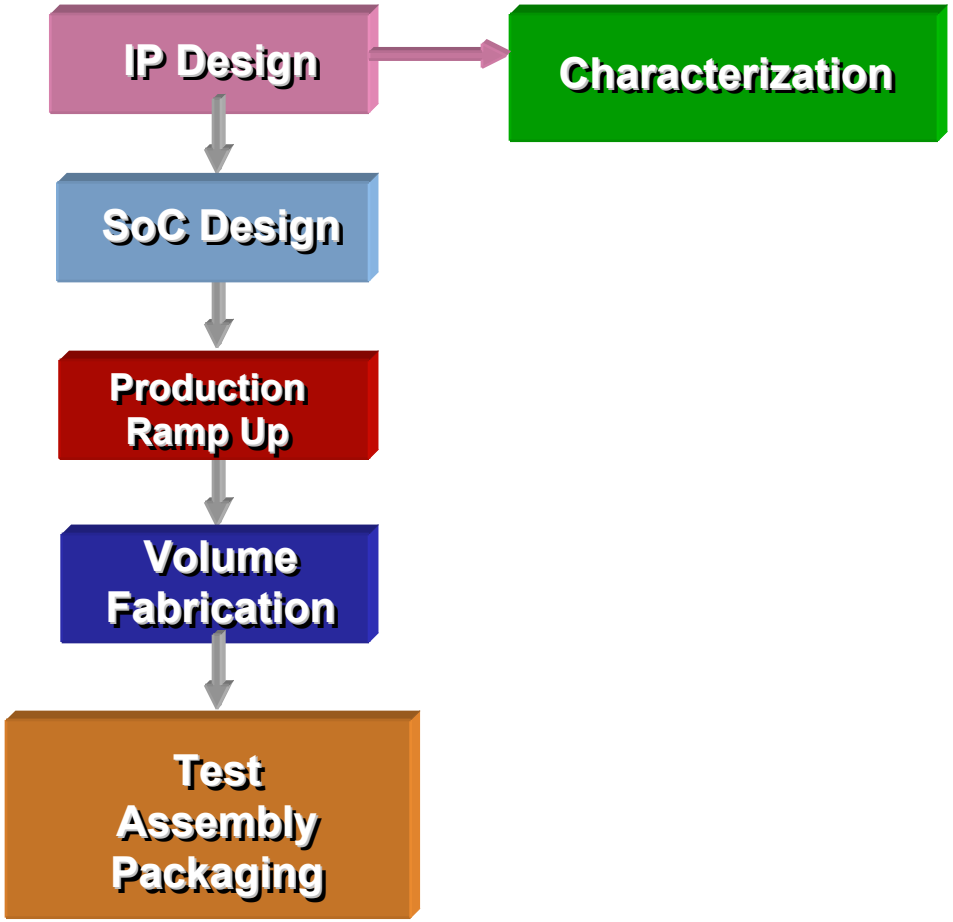

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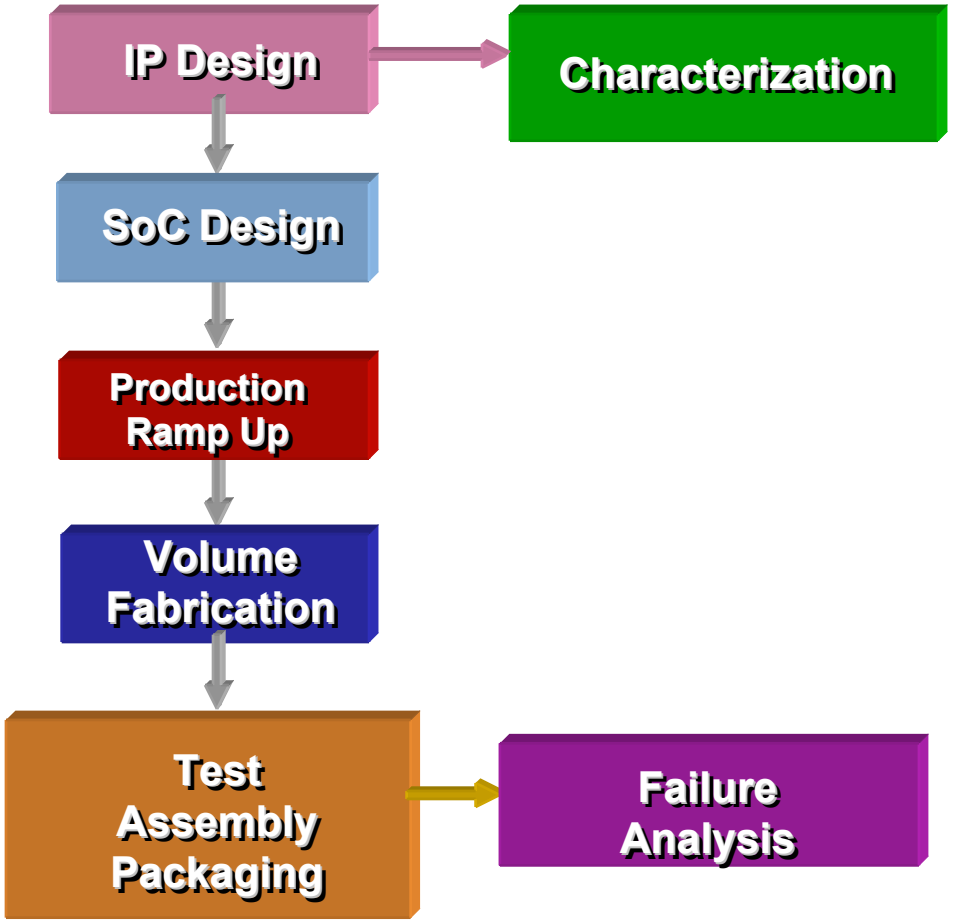

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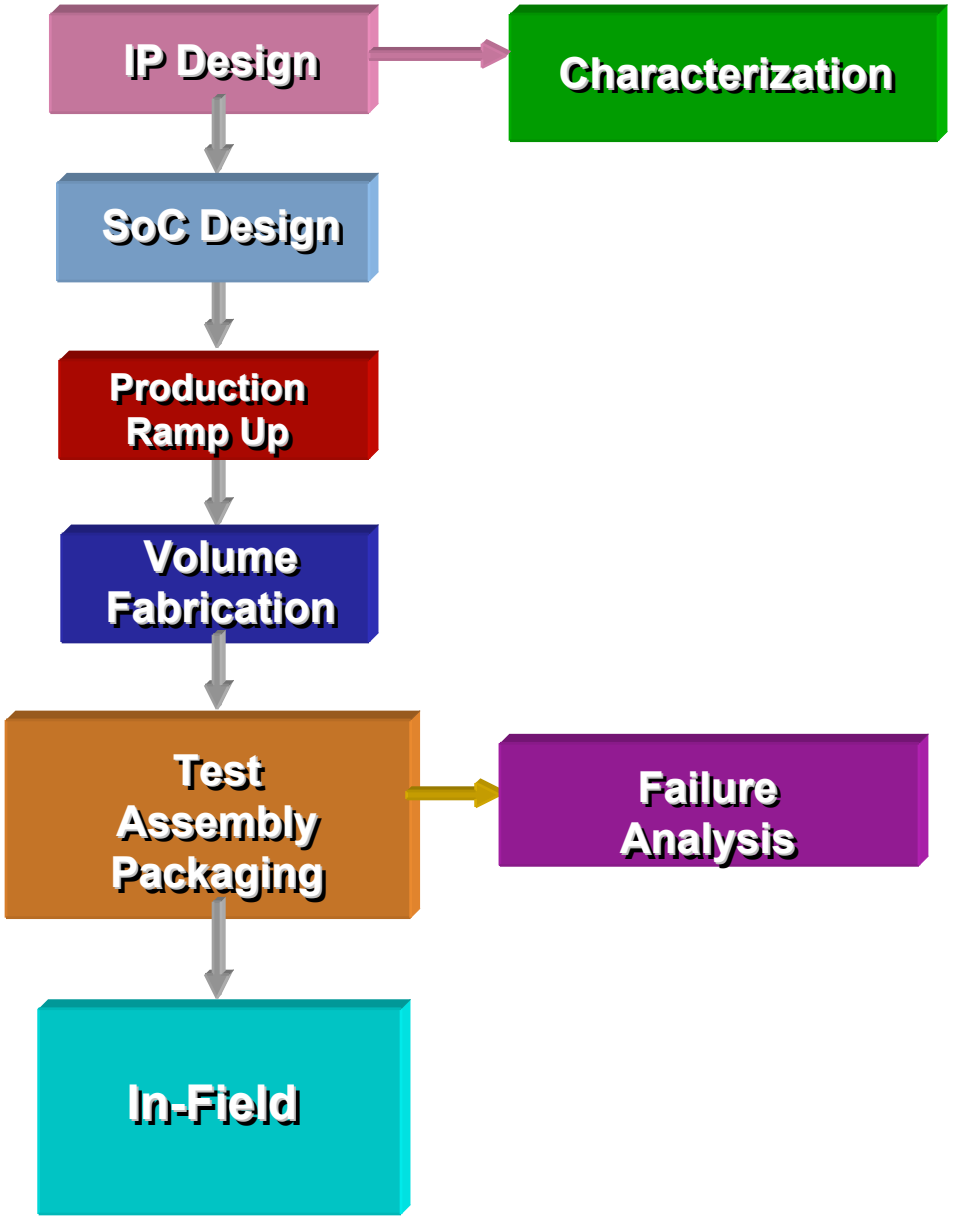
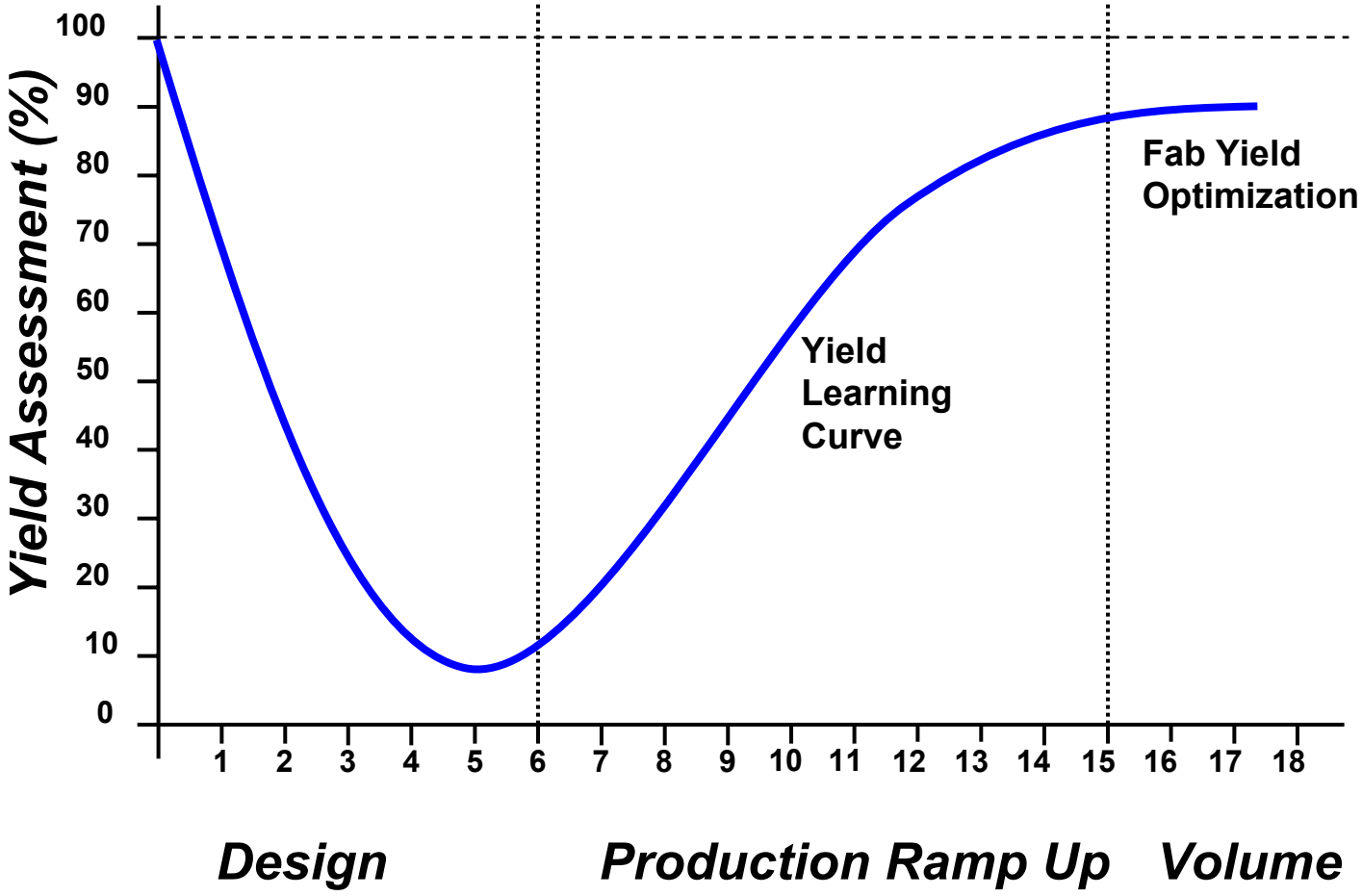


Yield Life Cycle Curve



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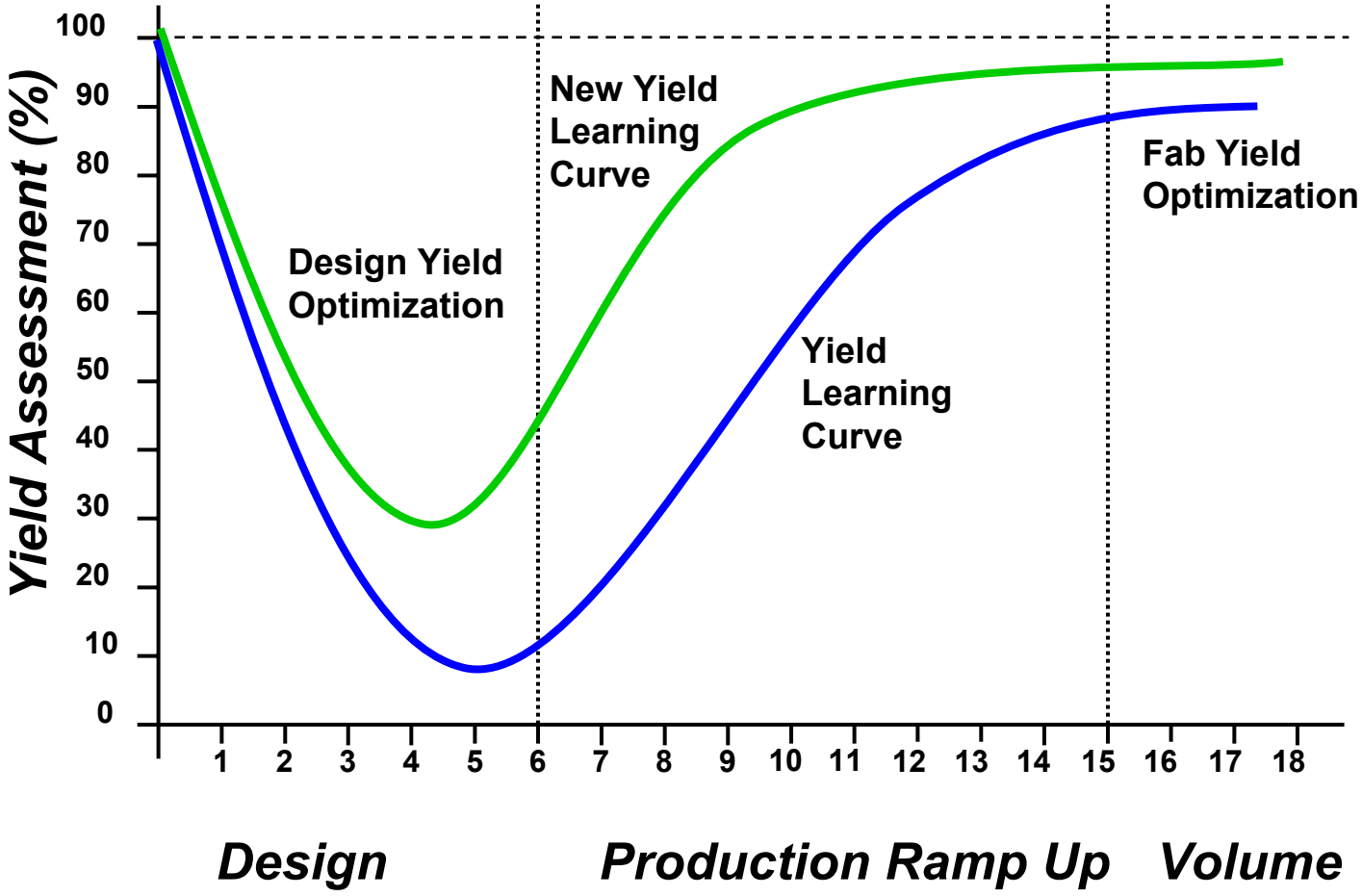

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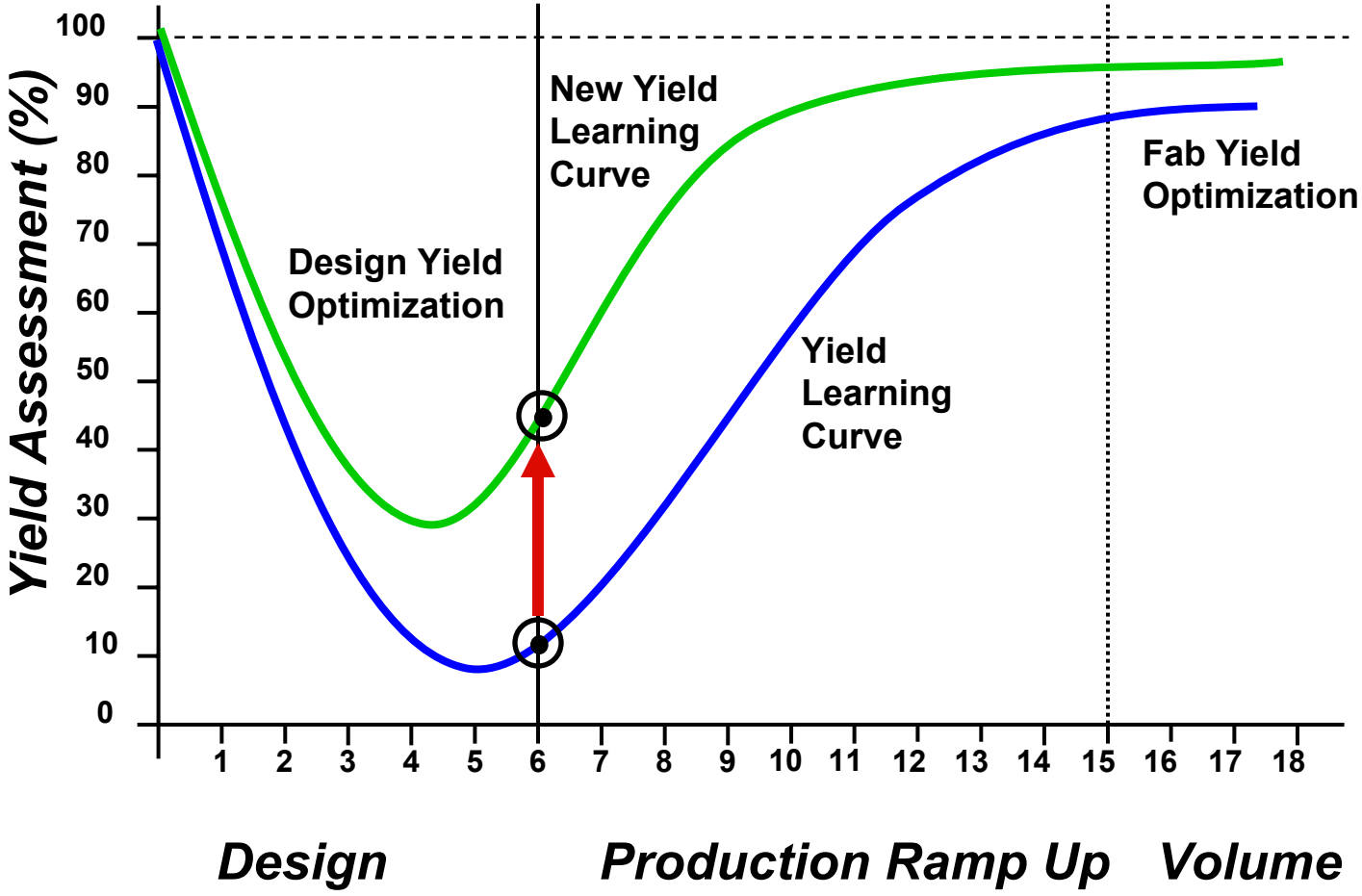

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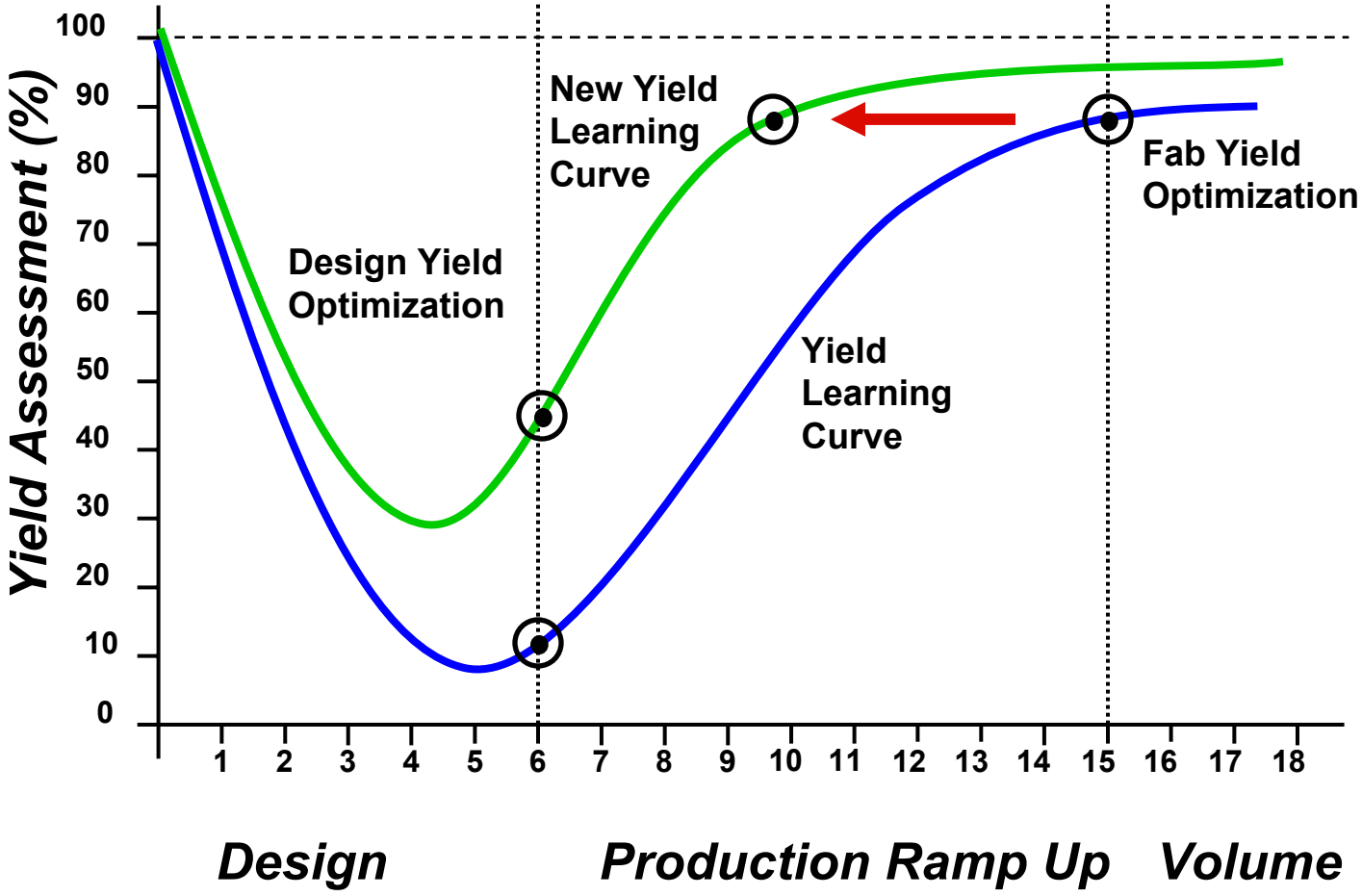

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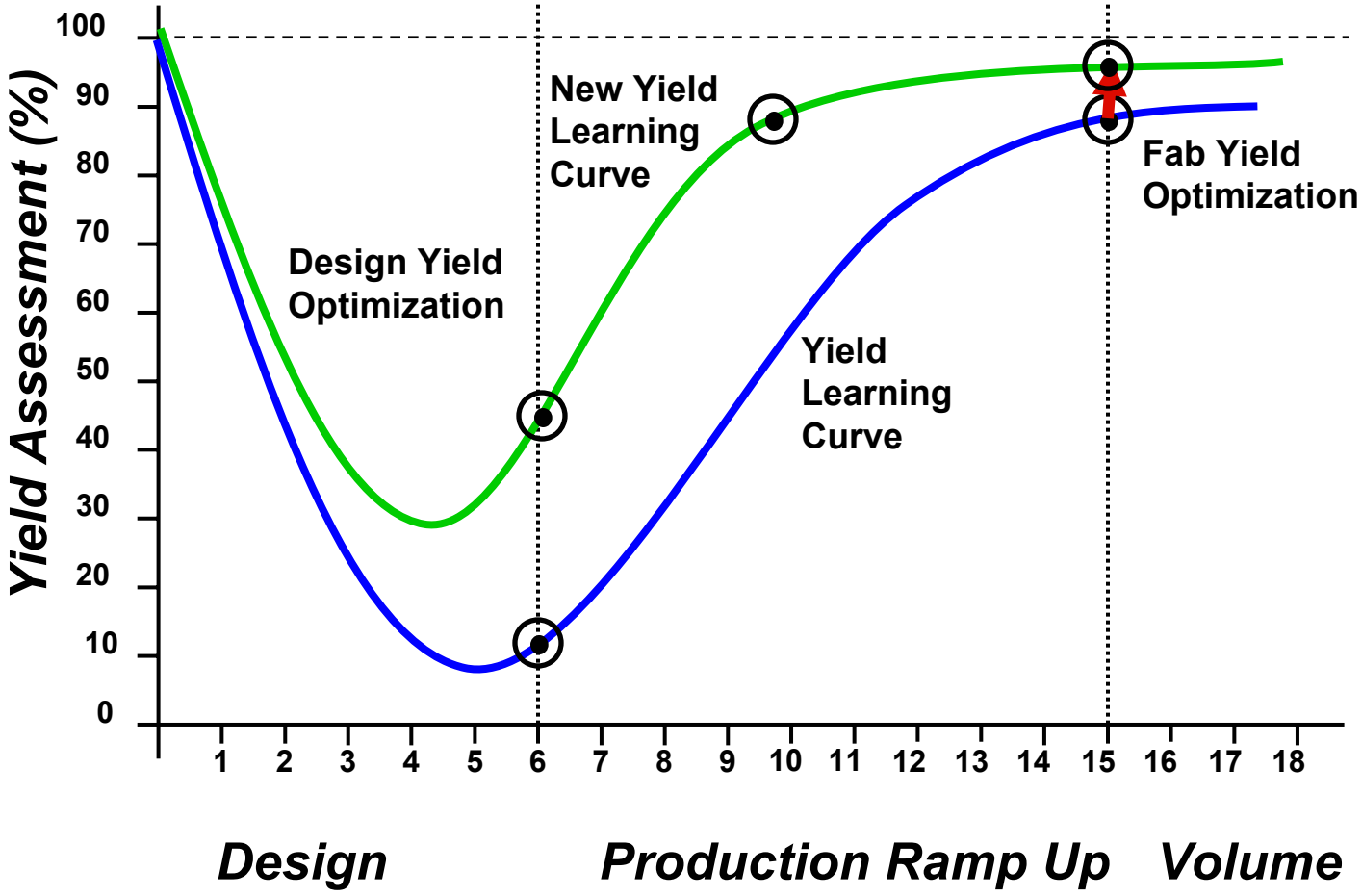
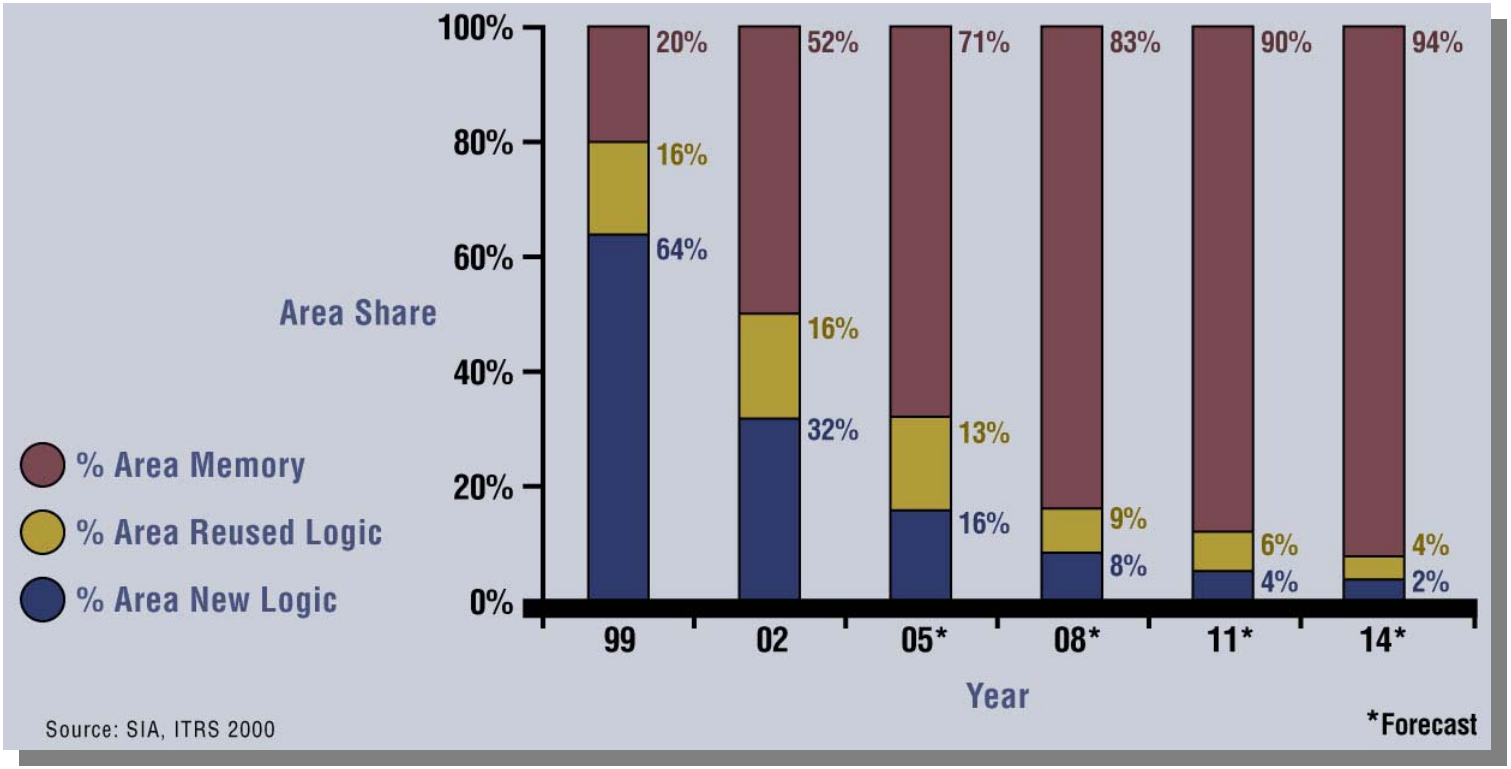


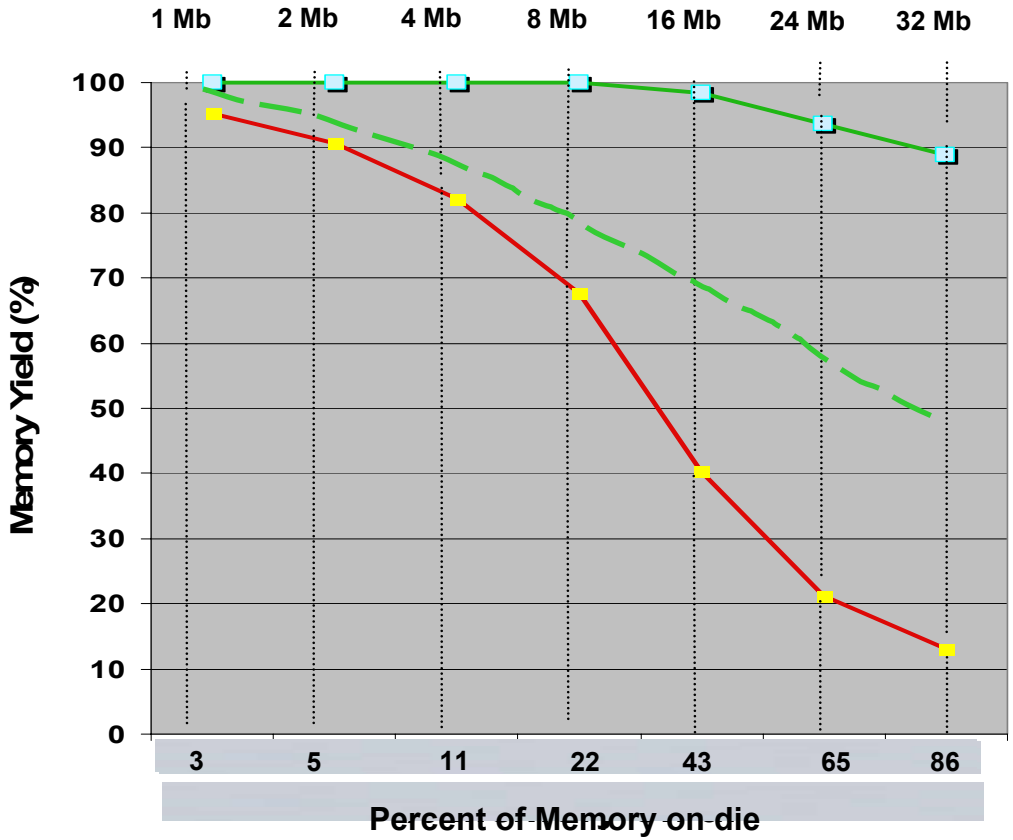
1. Yield Learning Challenge

- Semiconductor process evolving and introducing new material and techniques
  - result in new generation of yield limiting factors
- Small geometries
  - result in devices more susceptible to systematic and random defects and higher defect densities per layer
- Increased time-to-market pressure
  - result in chip volume production at lower yield level
- Disaggregated semiconductor industry
  - result in F-IP providers assuming yield optimization responsibility
- Need process monitor IP and yield prediction and optimization for each new design (IP and SoC)

2. Embedded Memory Challenge



2. Embedded Memory Challenge



Width of die in mm	12.00
Height of die in mm	12.00
Defect density for logic in # per sq. in.	0.4
Defect density for memory in # per sq. in.	0.8
Process technology	0.13 µm

3. Failure Analysis Challenge

- Traditional physical failure analysis steps -
  - Fault localization
  - Silicon de-processing
  - Physical characterization and inspection
- Small geometries result in –
  - Finding smaller more subtle defects
  - Tighter pitches require greater spatial resolution
  - Backside analysis due to metal layers & flip-chip
- Need to gather failure data using diagnosis IP and analyze obtained data by off-chip fault localization methodologies and tools

4. High Performance Challenge

- Increased performance require increased accuracy for proper resolution of timing signals
- Semiconductor on-chip speed improved 30% per year, test accuracy improved 12% per year
  - Tester timing errors approaching cycle time of faster device
  - Yield loss due to tester inaccuracy (extra guard-bending performed at test stage)
- Need for measuring and analyzing time specifications using embedded timing probes with high accuracy

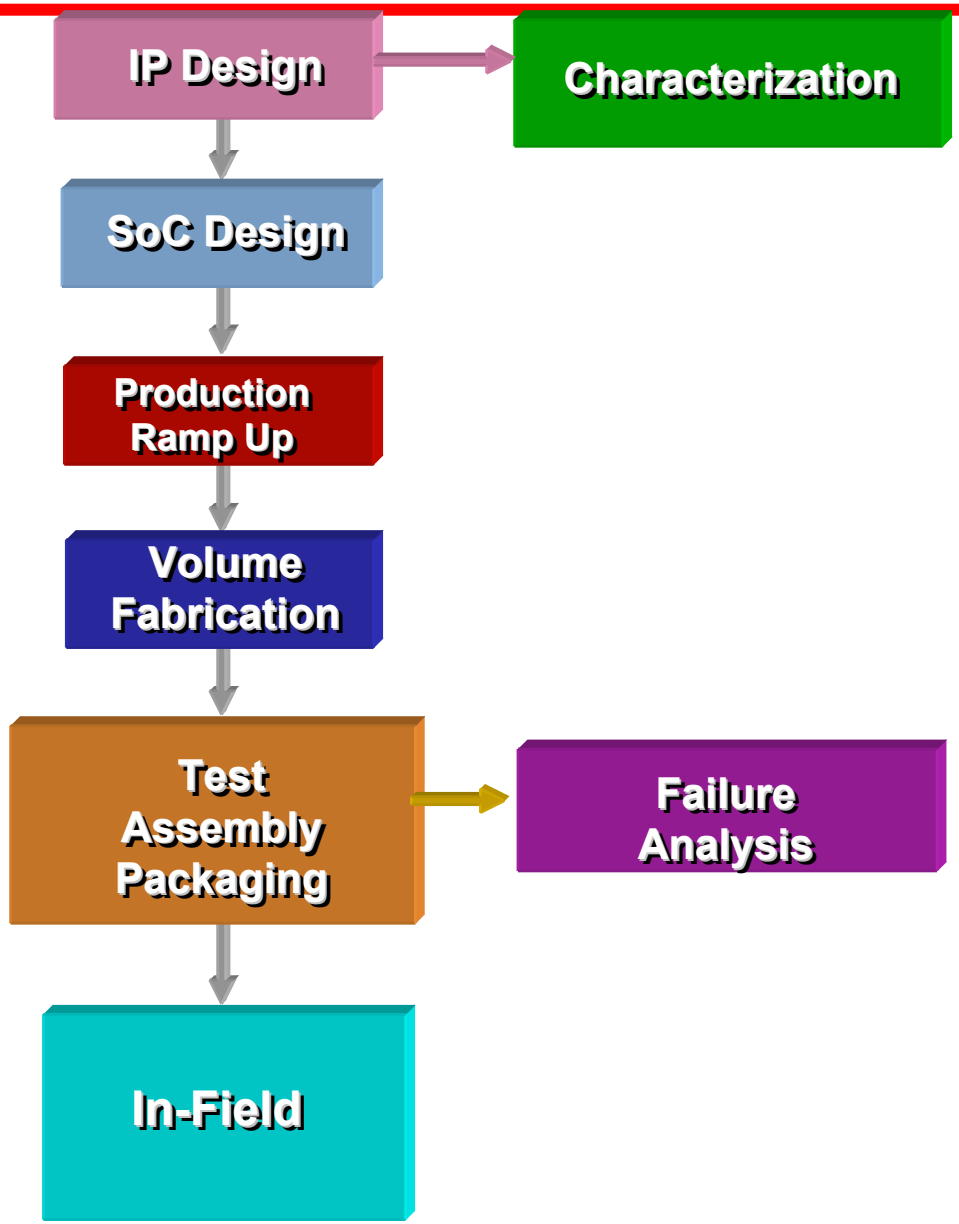
5. Transient Error Challenge

- Smaller geometries and reduced power supplies result in reduced noise margins
- Soft errors,timing faults, crosstalk are major signal integrity problems
- SoC needs self correcting, i.e. embedded robustness, engine in order to resist to this challenge

Yield Optimization Loops

- Need for Advance yield optimization solutions
- Introduced at different stages of chip realization flow
- Yield optimization feedback loops – comprised of three steps
  - Detection, Analysis, Correction
- Three step loops either reside completely off-chip, partially on-chip/off-chip or embedded on-chip
- Examples of yield optimization feedback loops

Yield Optimization Loops



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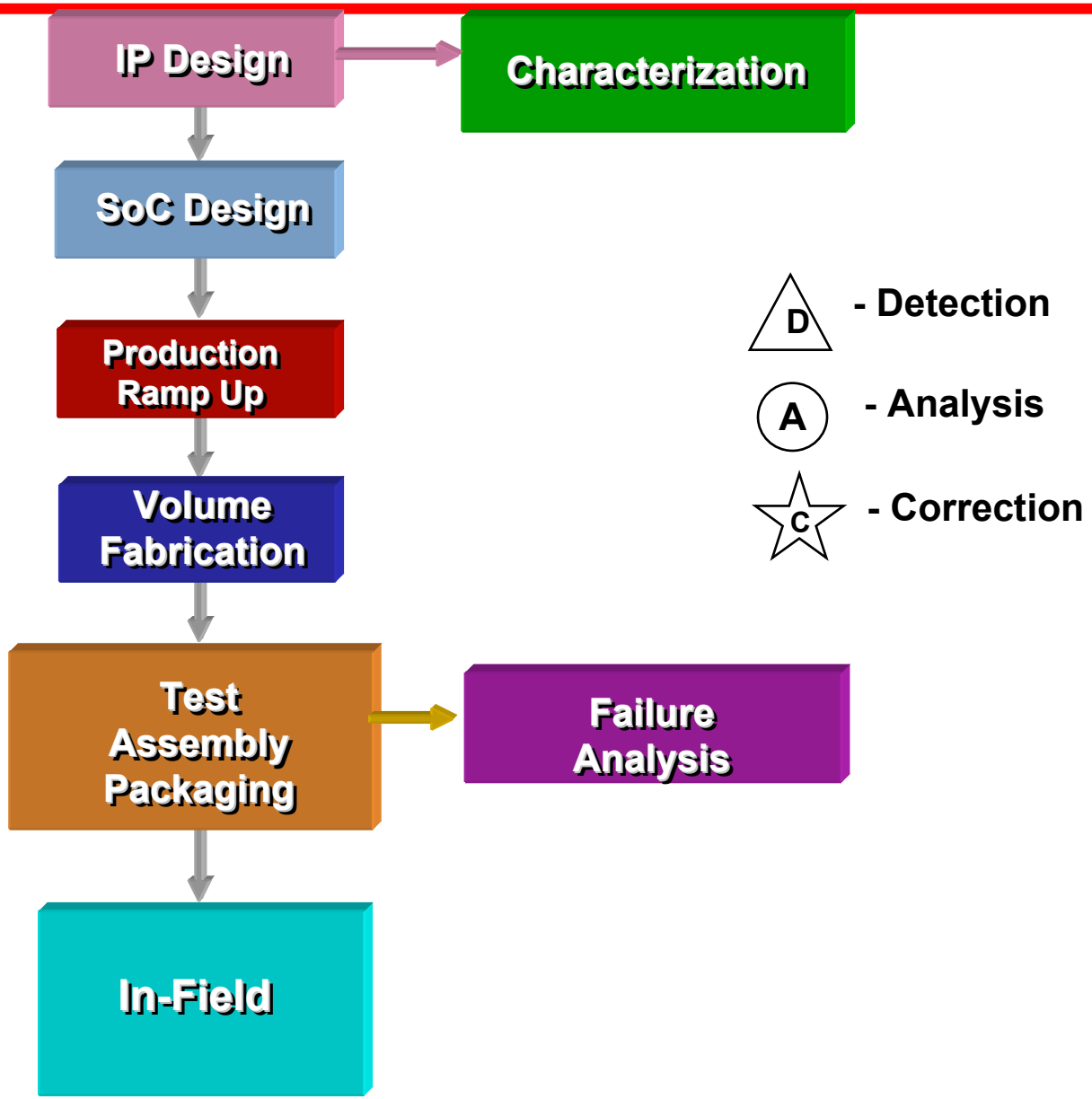

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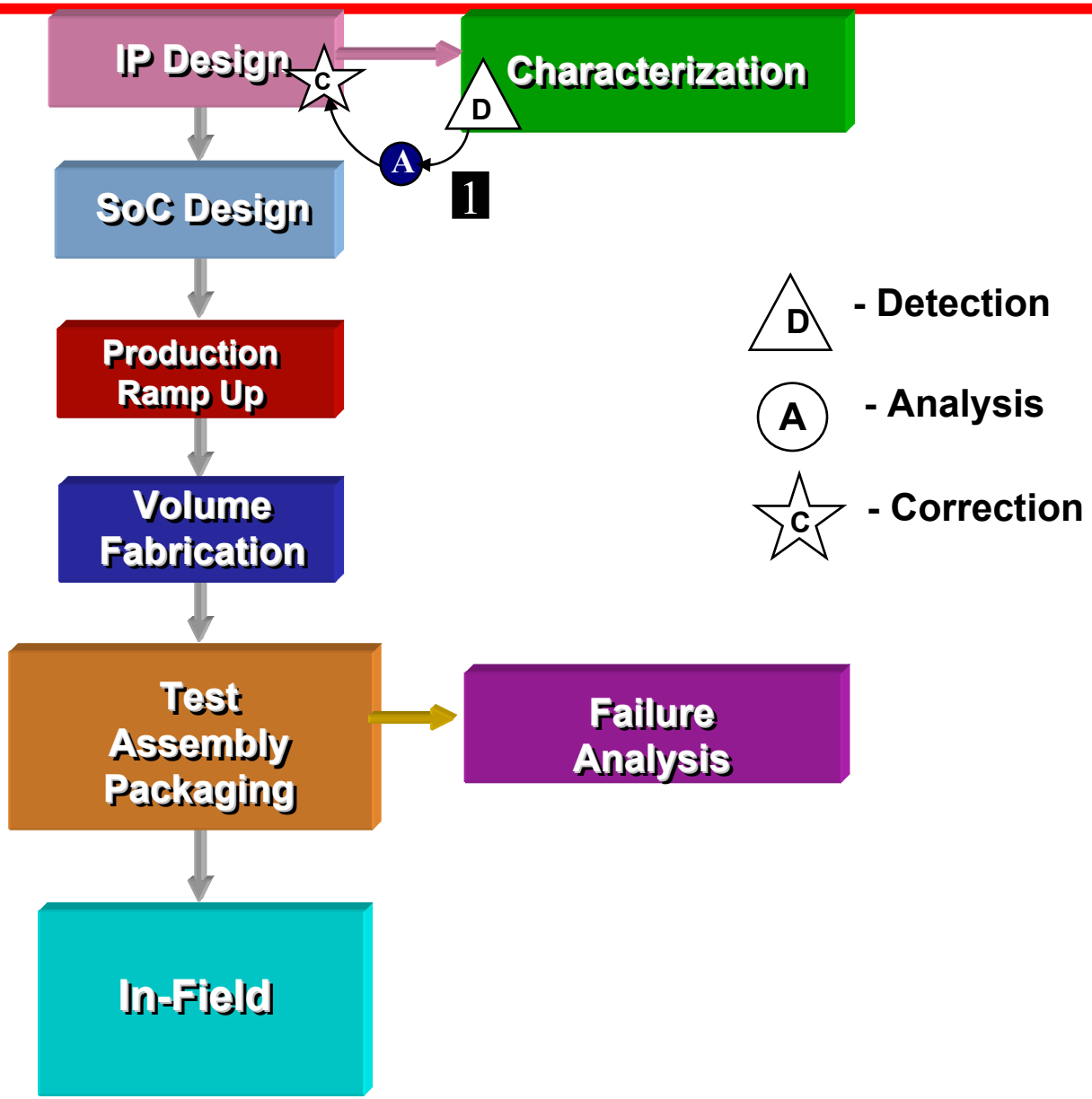

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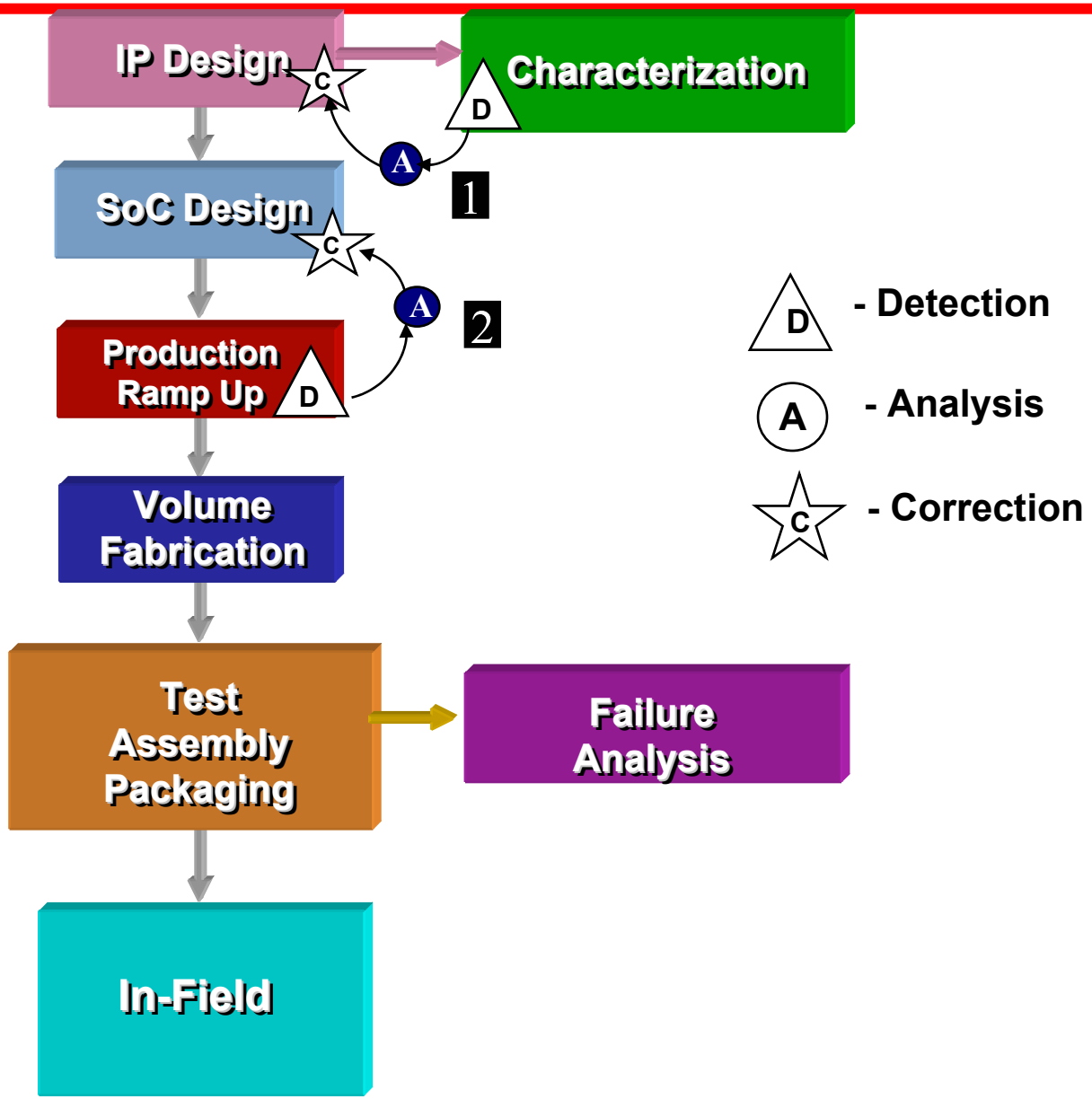

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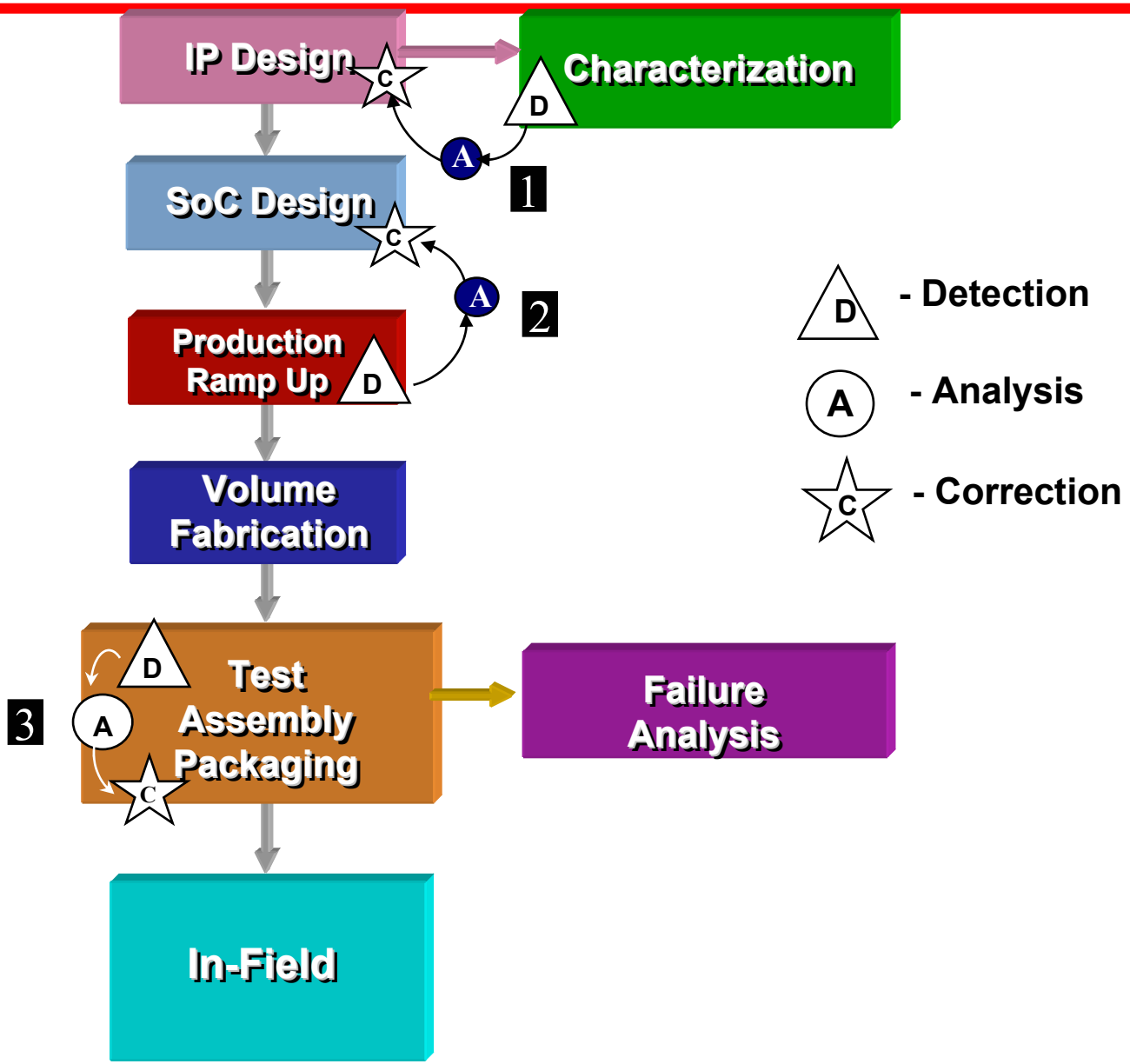

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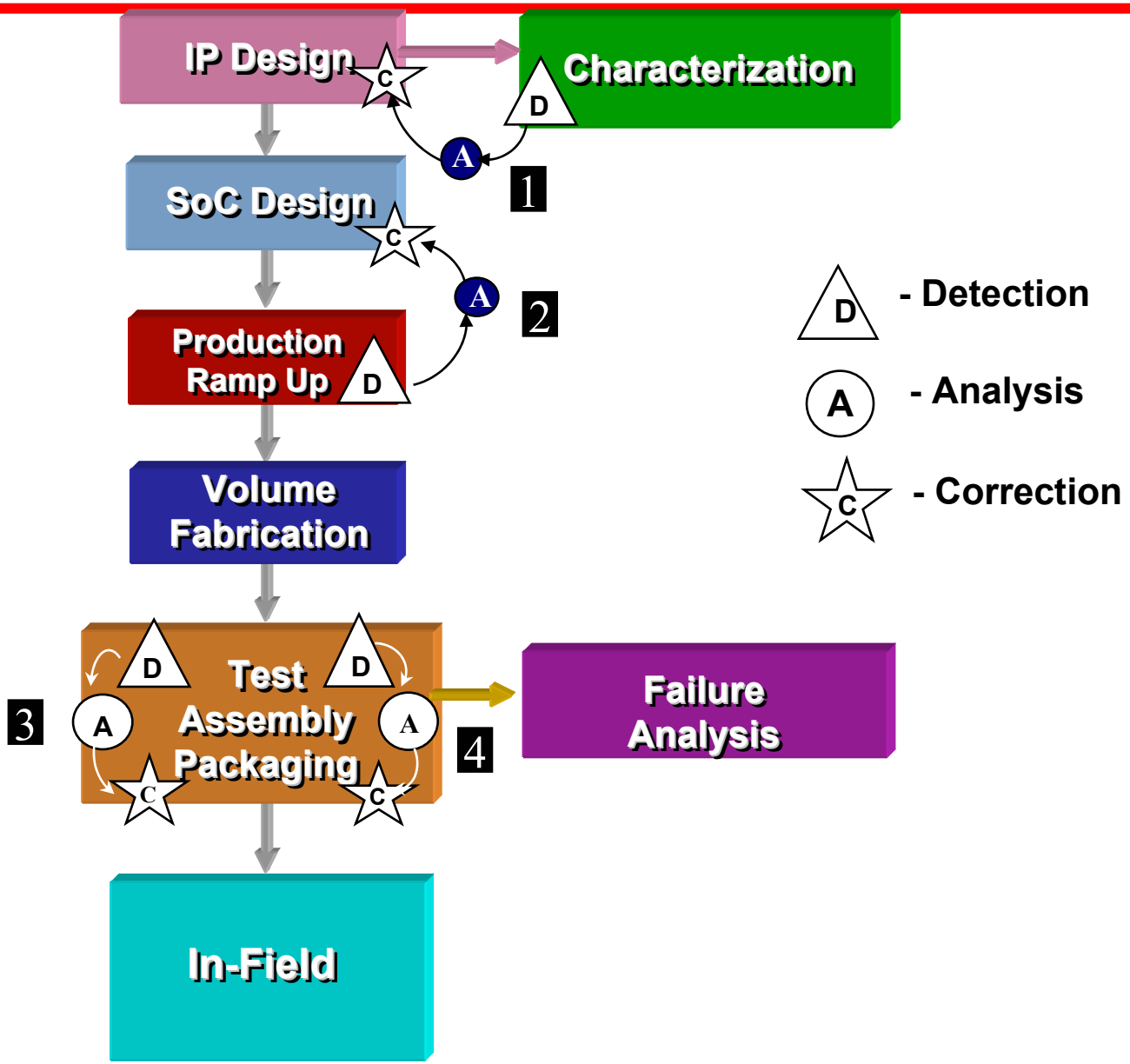

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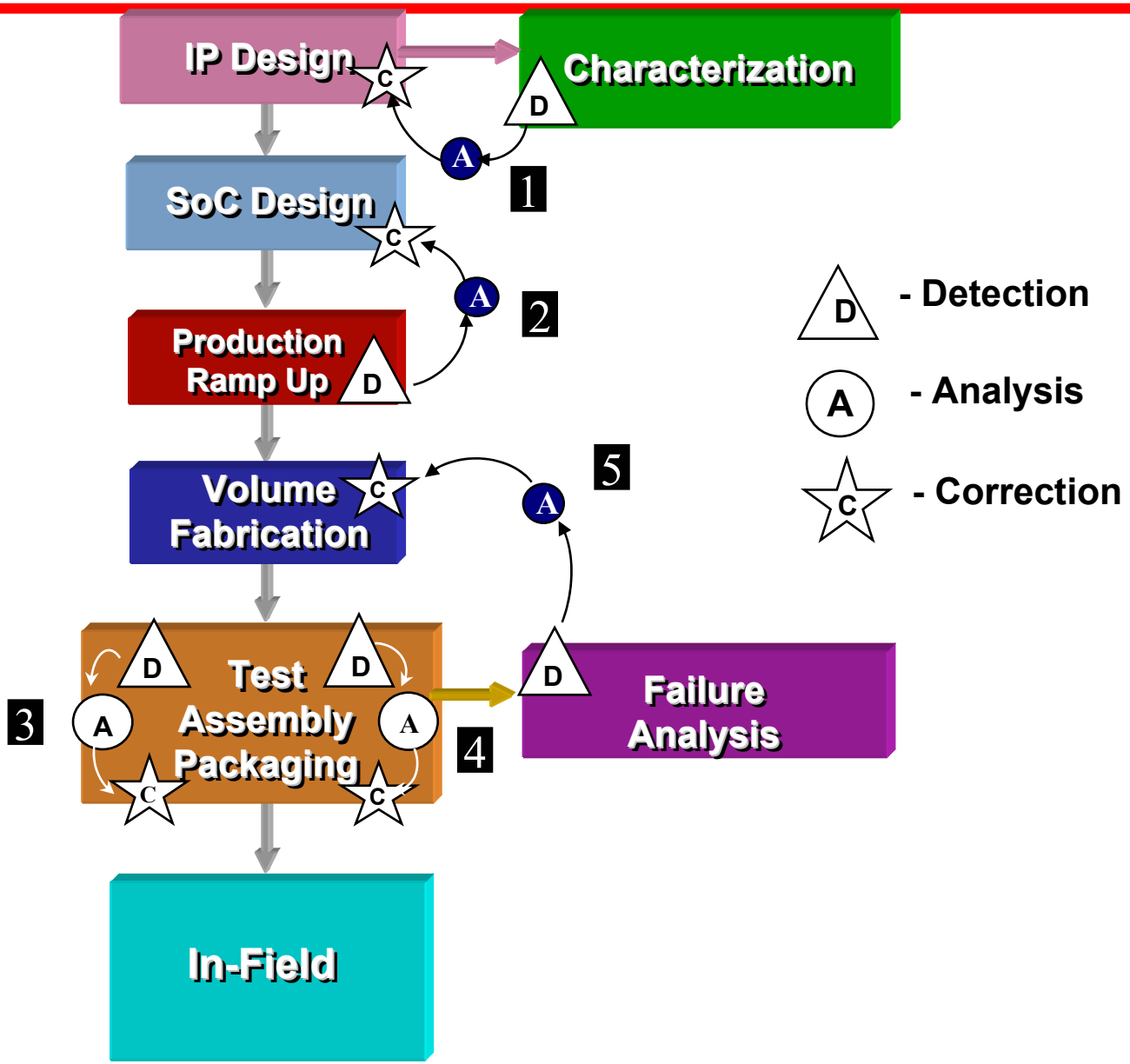

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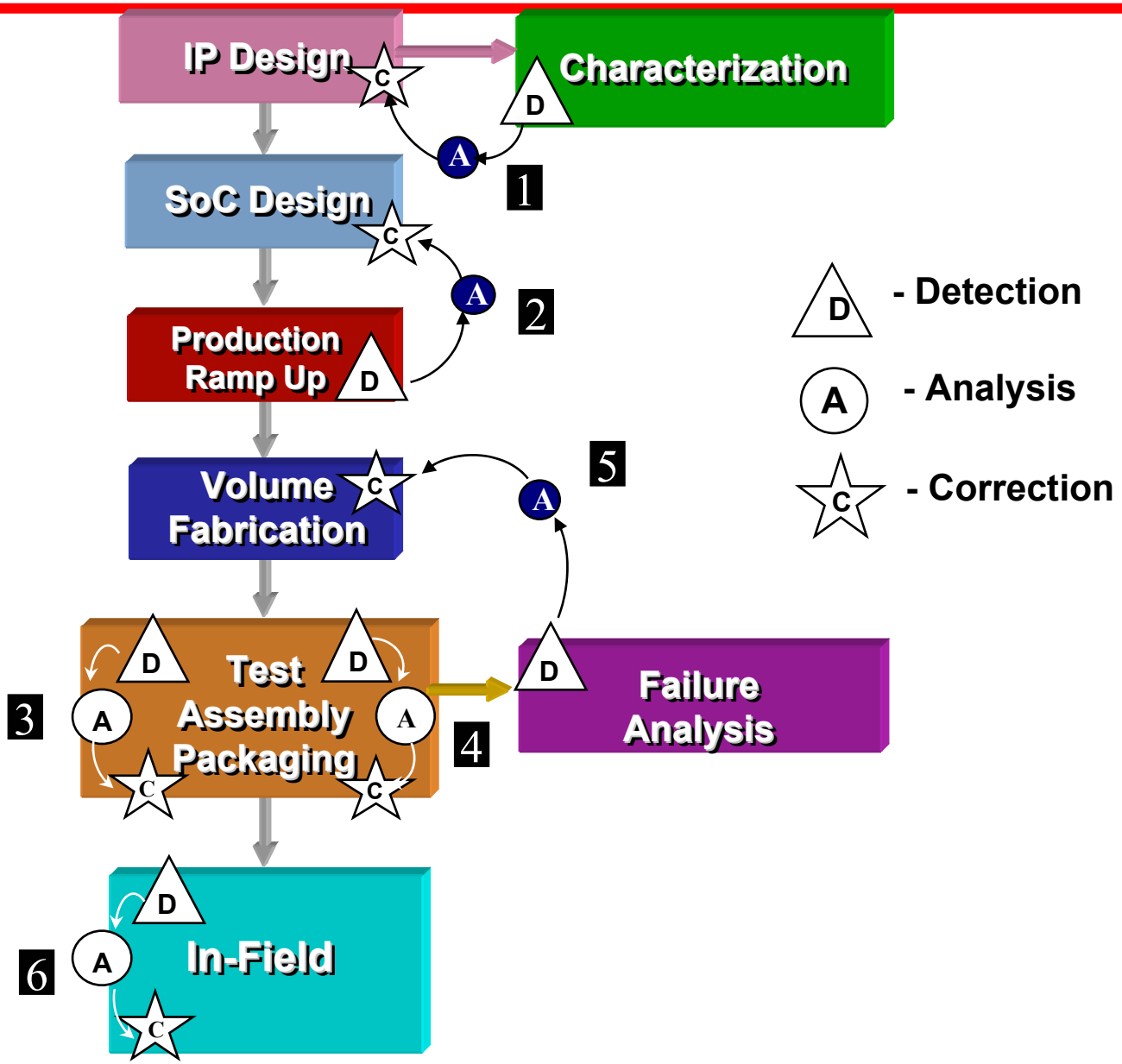

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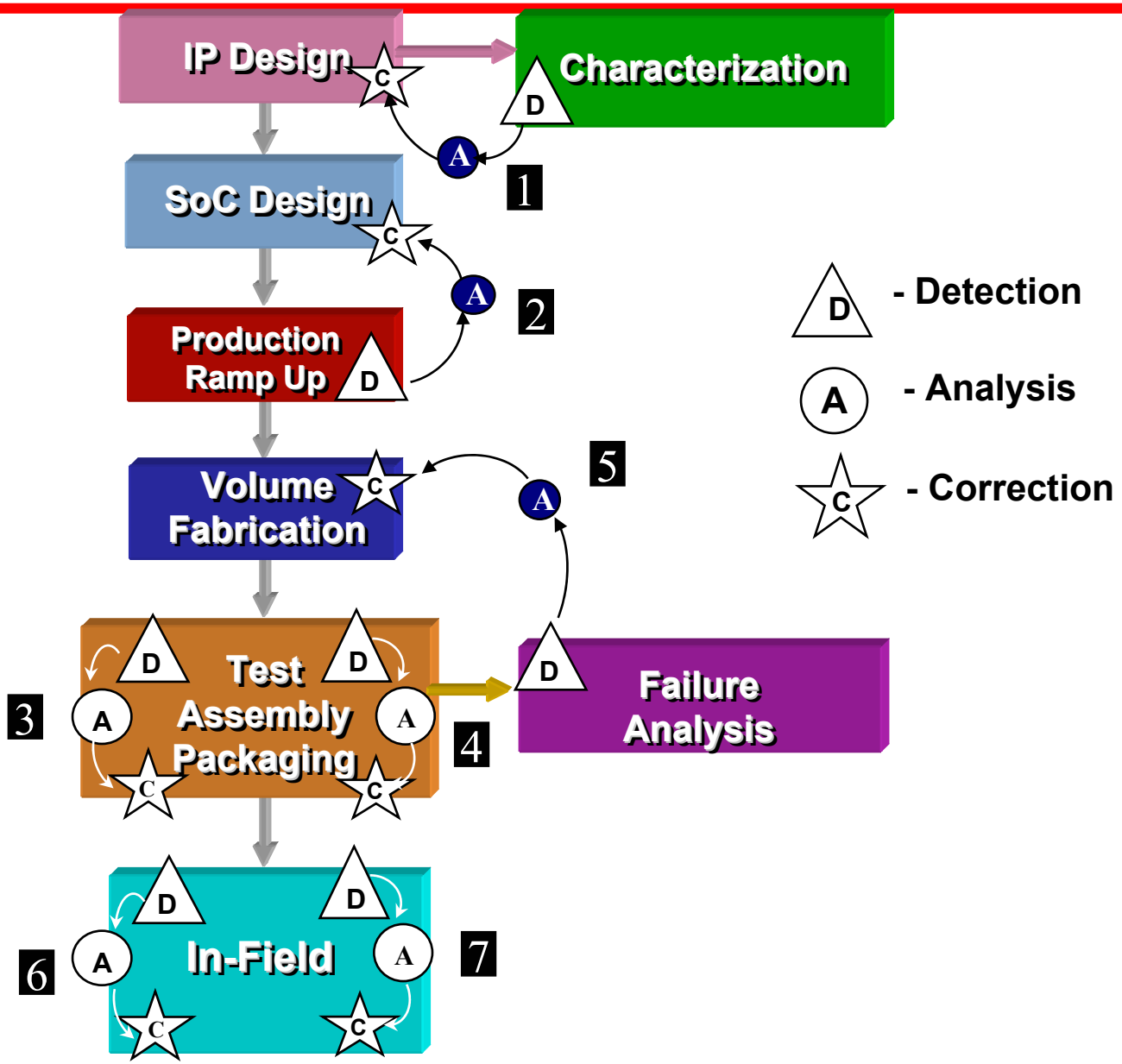
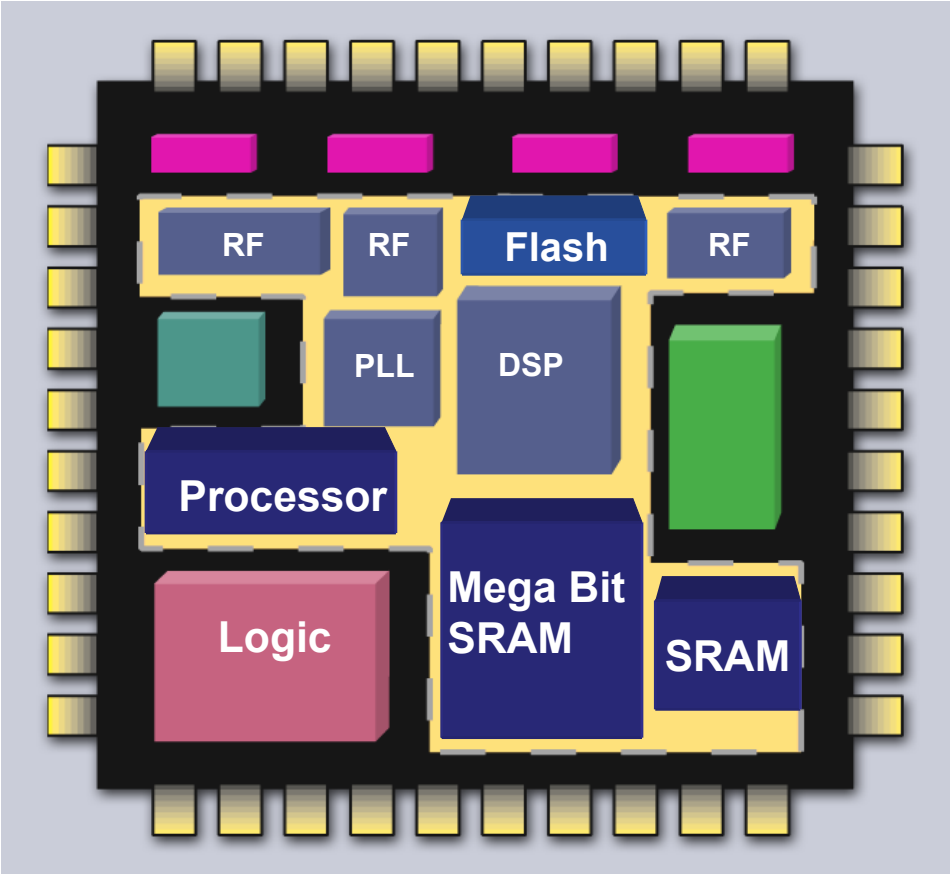


Functional IP in SoC

Multiple Functional IP (F-IP) types have been absorbed into single SoC design



Infrastructure IP in SoC

- Transparent to normal functionality of SoC (not functional IP)
- Ensures manufacturability and lifetime reliability of SoC
- Basic types of Infrastructure IP include:
  - IP for process monitoring
  - IP for testing
  - IP for diagnosis and debug
  - IP for repair
  - IP for characterization & measurement
  - IP for robustness and fault tolerance

Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design

Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors

Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer

Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level

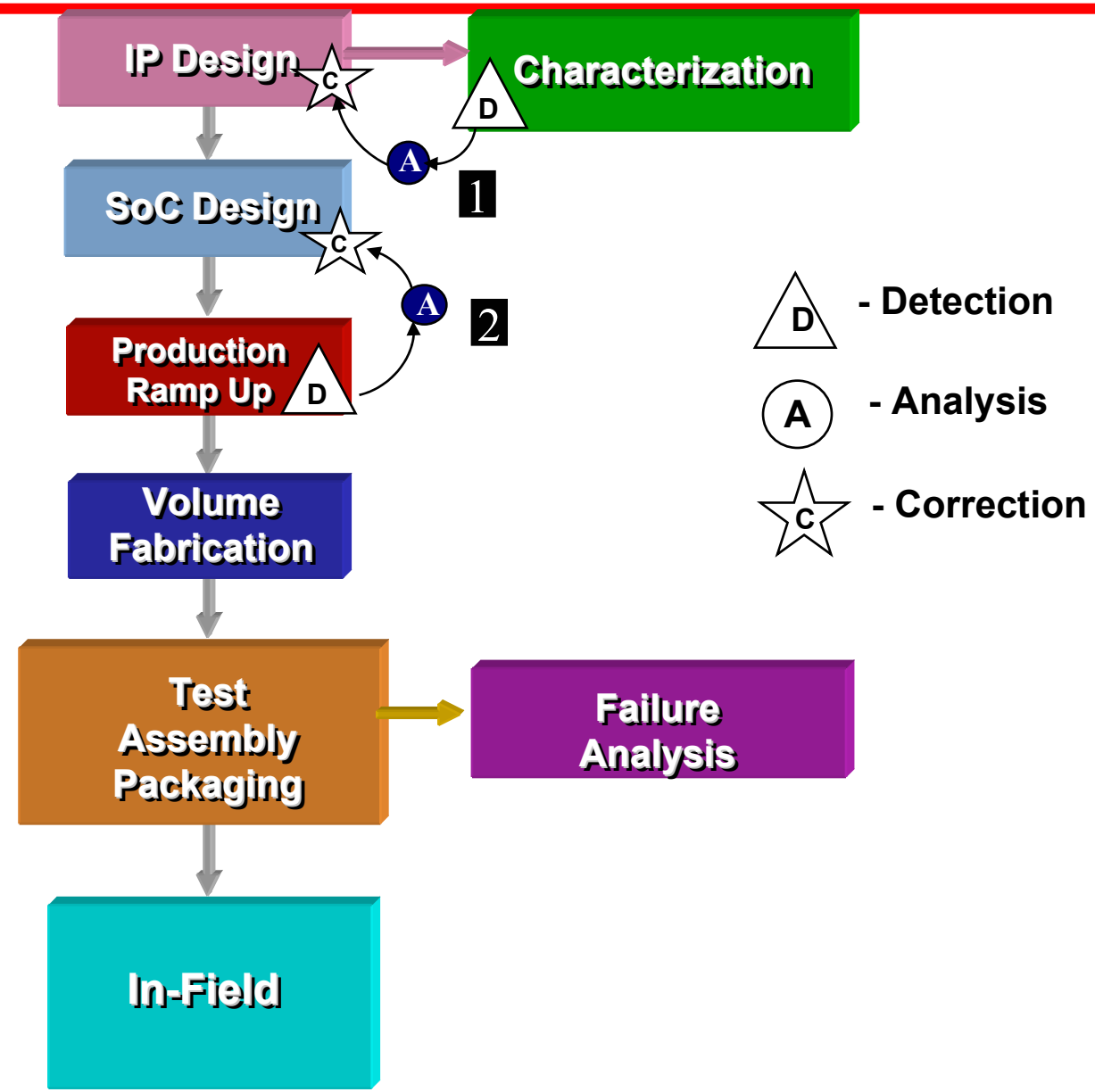
Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level
  - Embedded I-IP distributed over F-IP

Infrastructure IP in SoC

- Infrastructure IP absorbed into Soc design
  - External equipments and sensors
  - Embedded I-IP on Wafer
  - Embedded I-IP at SoC level
  - Embedded I-IP distributed over F-IP
  - Embedded I-IP integrated into F-IP
- Resource partitioning and I-IP at multiple levels
- Examples of Embedding I-IP to create YOL

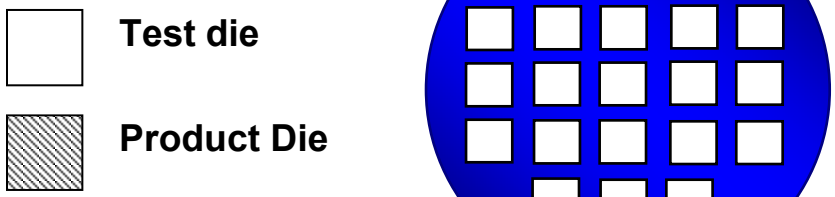
1. Embedded Process Monitor IP

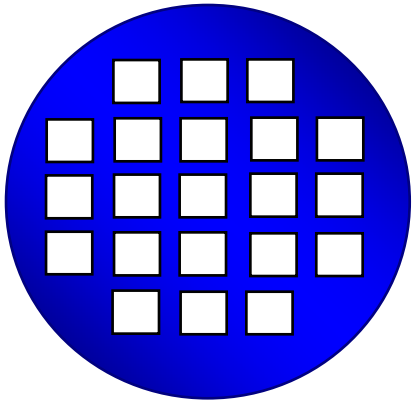


1. Embedded Process Monitor IP

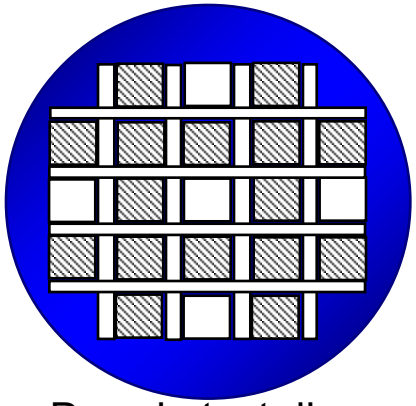
- Passing DRC does not guarantee high yield
- D-component of feedback loop is I-IP
  - Monitor process characteristics
  - Collect device attributes
- Known as: test vehicle or test die
- Process Monitor IP used during process development and/or later during production
- Process Monitor IP may be test die (full chip), scribe or embedded IP in SoC

1. Embedding Process Monitor IP

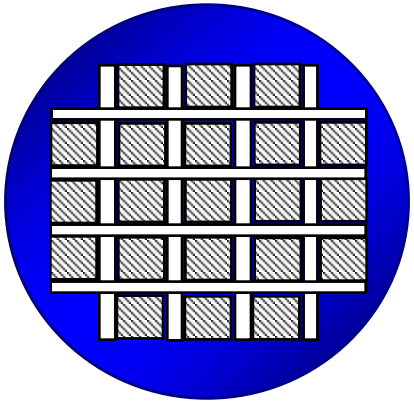




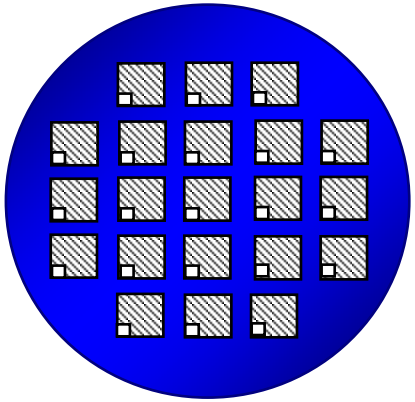
Process development
I-IP



Drop-in test die
with scribe



Scribe only



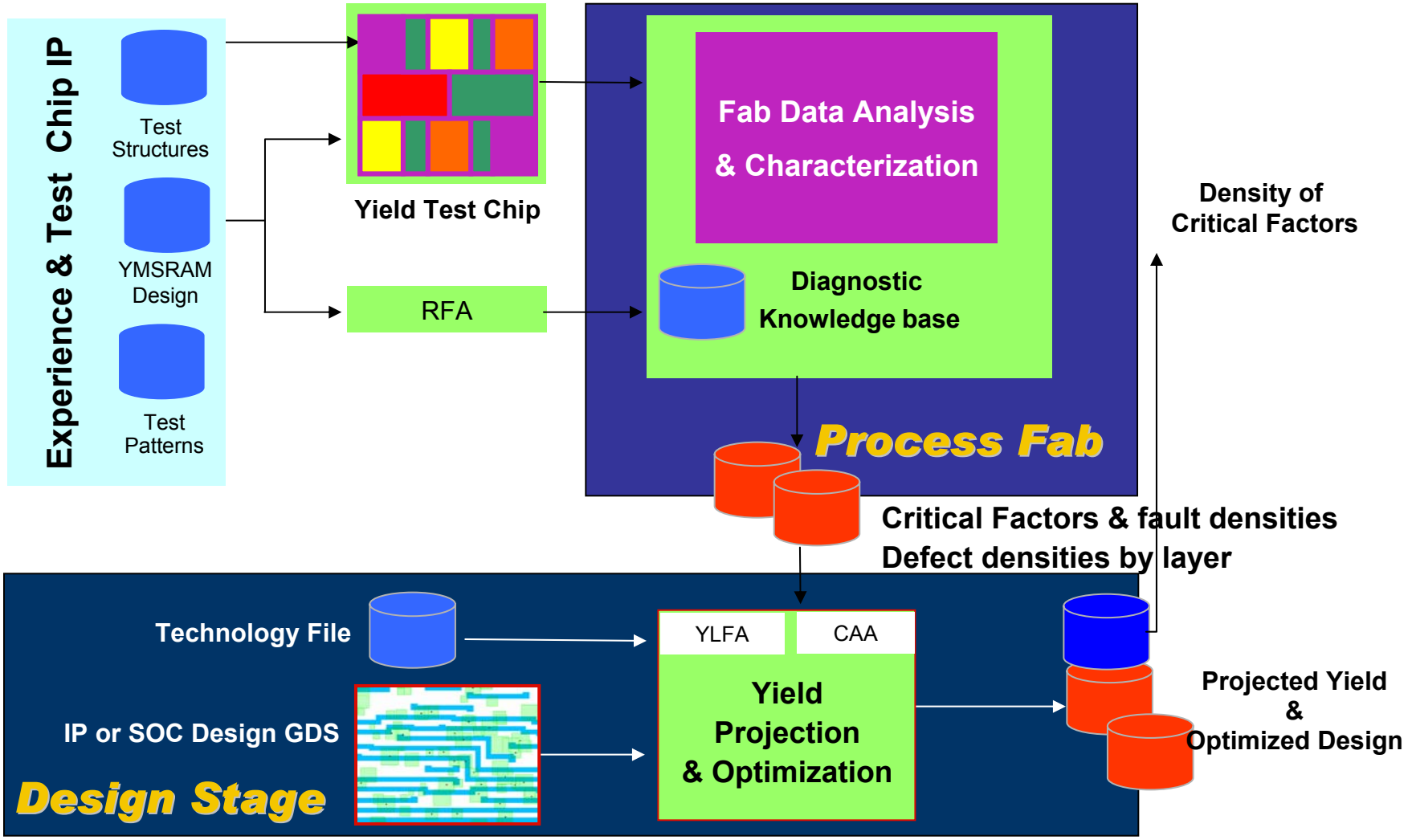
Product die with embedded IP

Source HPL Technologies

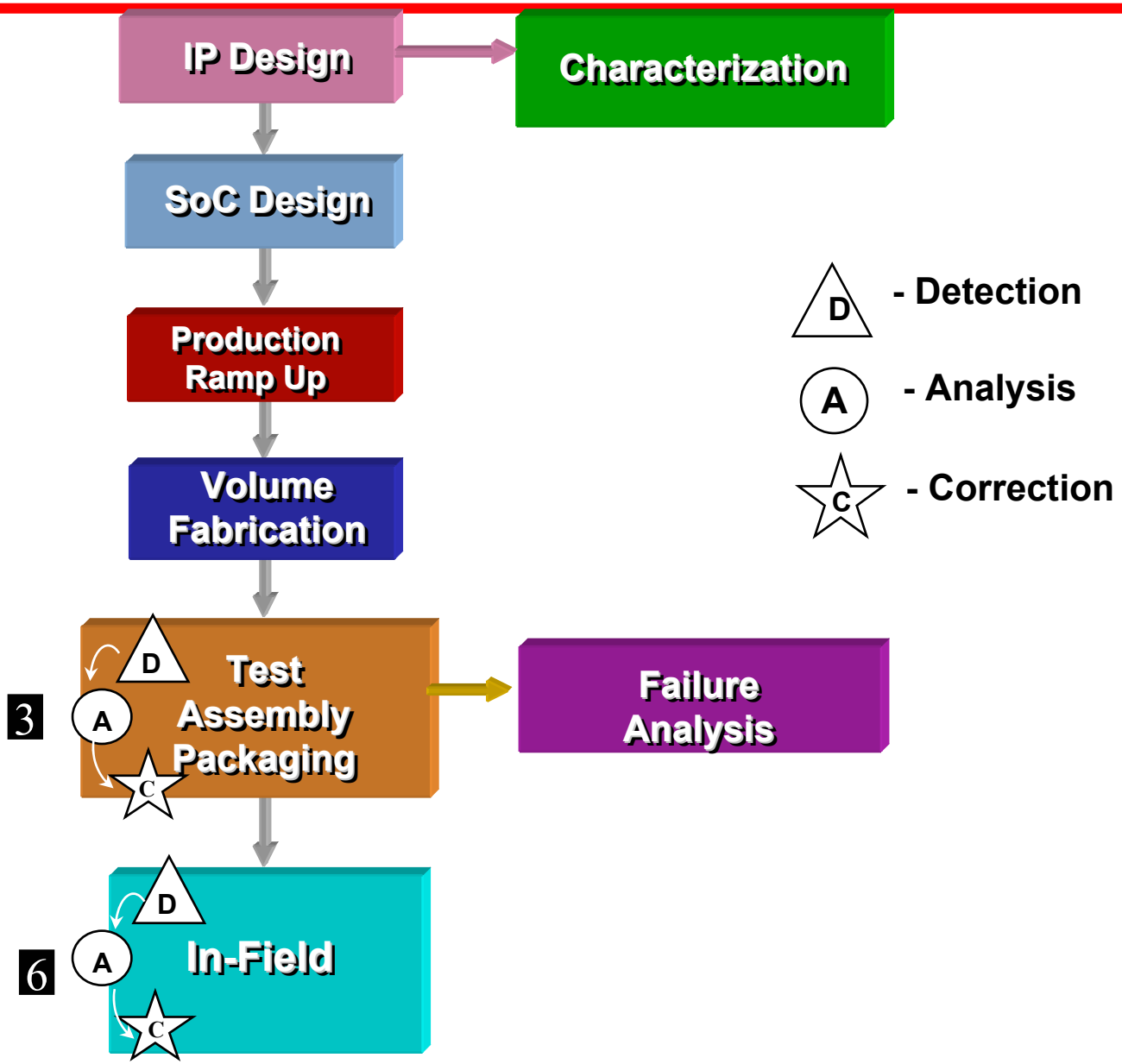
1. Embedded Process Monitoring IP

- Use information and knowledge about process to predict yield of a given design (IP or SoC) before it is committed to silicon (A- component)
- Identify weekest links in design
  - Block, IP, layer, design structures
- Yield Optimization: improve design (IP or SoC) by modifying week links at GDS level (C- component)

1. Using Process Monitor IP

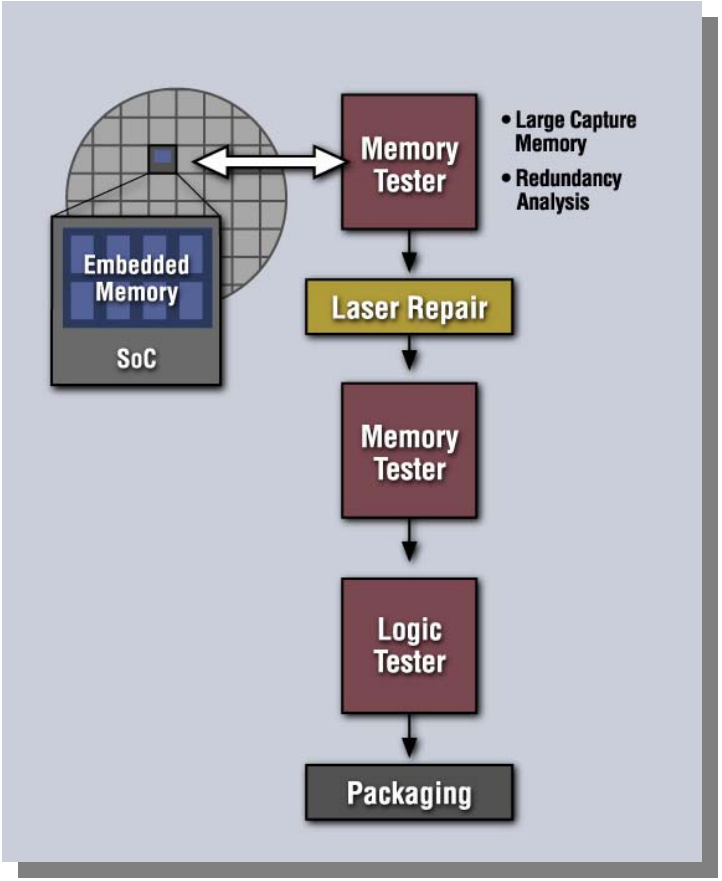


2. Embedded Test & Repair IP



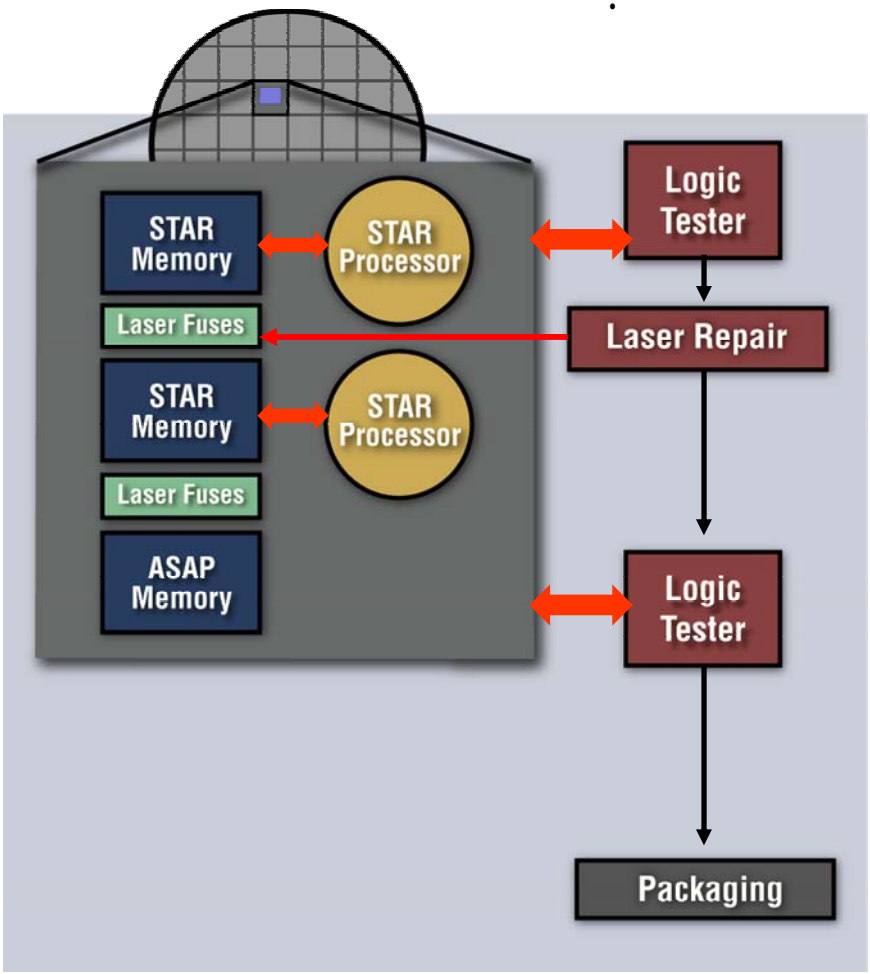
2. Limited I-IP for Test Only

- Barriers: Manufacturing
  - Cost
    - $3-7 Million equipment cost
    - 40% of manufacturing cost
  - Access
    - Providing test access increases die size



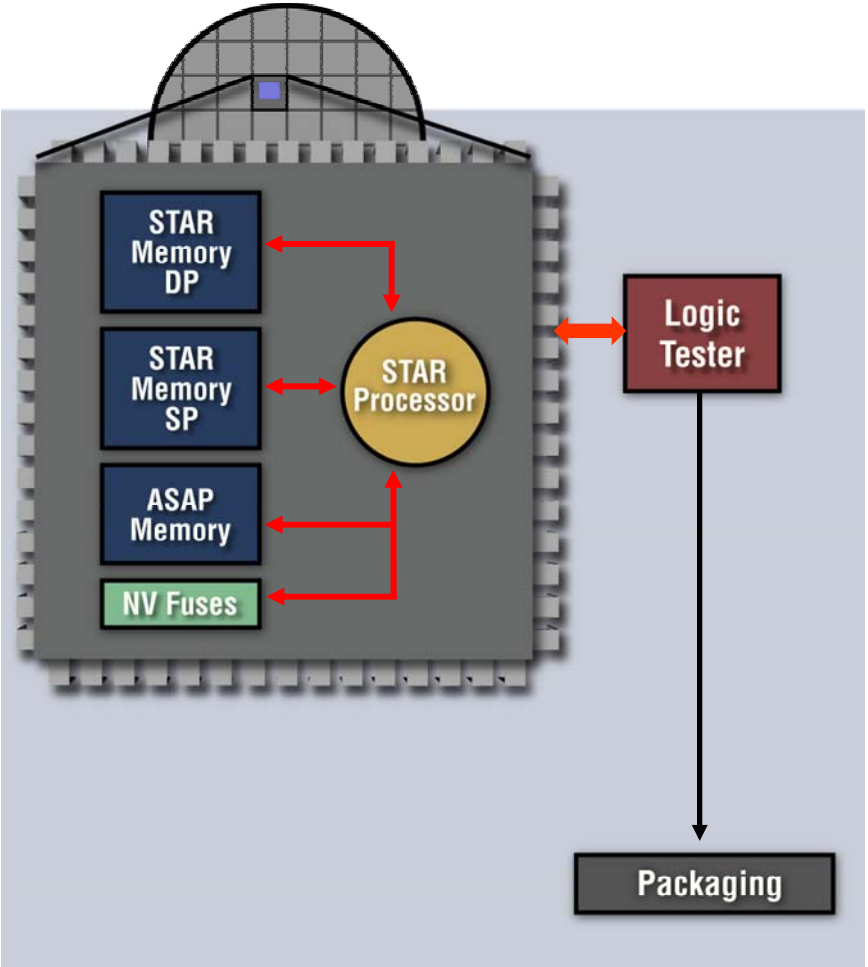
2. I-IP for One Time Repair

- External Memory tester need eliminated
- External bit map storage eliminated
- External redundancy analysis software eliminated
- High yield achieved because of integrated solution

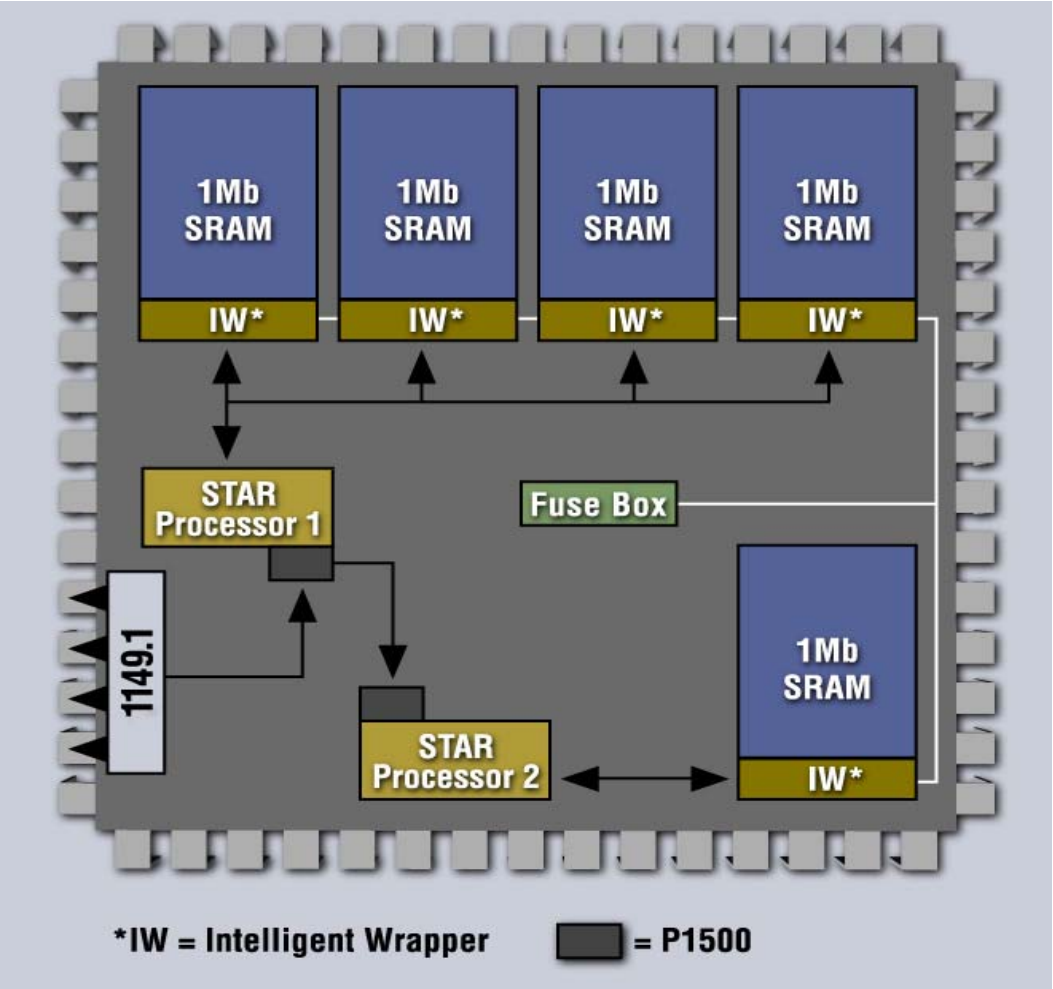


2. I-IP for Multi-Time Repair

- External repair equipment eliminated
- Overall manufacturing cost reduced
- Efficiency of repair increased (PVT corner conditions repaired)
- Efficient of area & performance improved



Composite IP for Embedded Memories

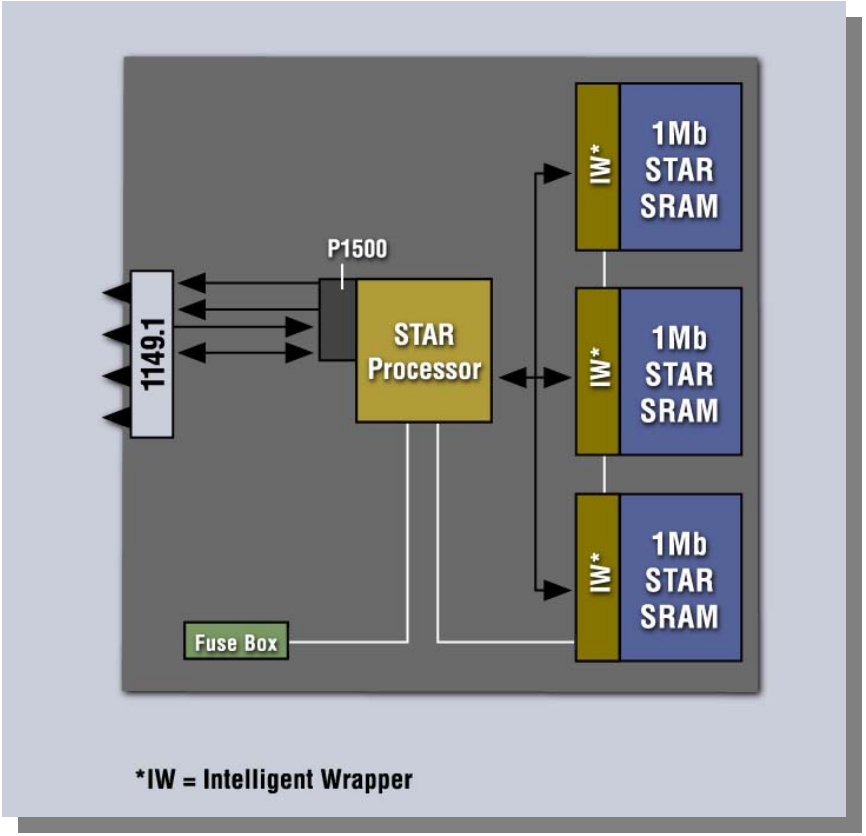


2. Quality & Reliability

- Highest defect coverage
  - Very deep submicron impact on defectivity in embedded memories
- Highest repairability levels
  - Complex redundancy mechanisms

2. Distributed I-IP for ET&R

- Built-in memory self-test
- Defect Analysis
- Redundancy allocation
- Repair
- Reconfiguration data download
- Retest

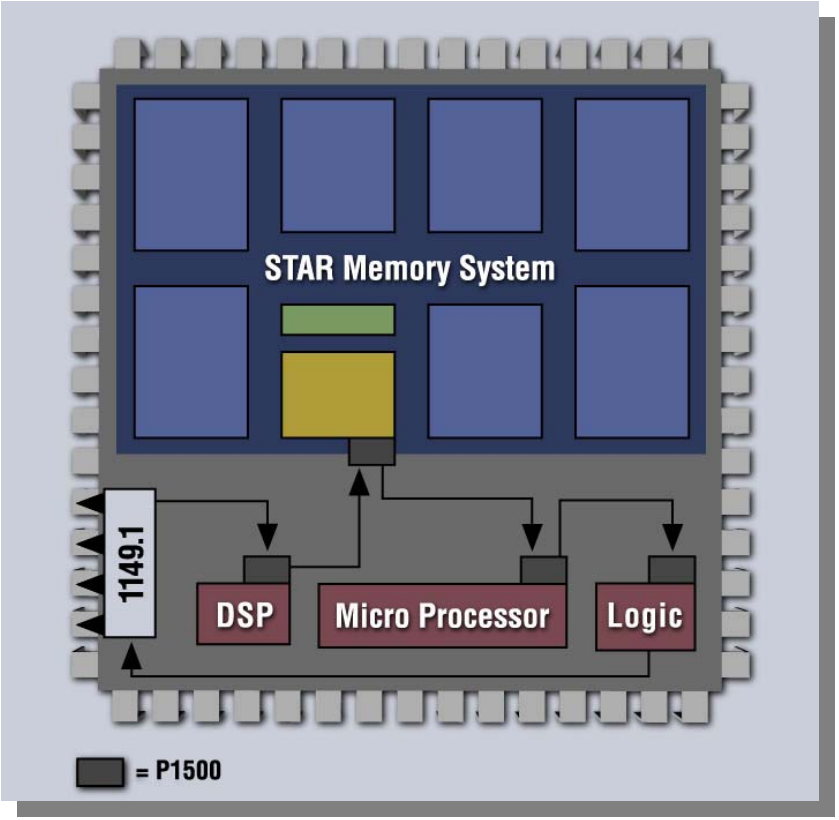


2. I-IP Effect on Yield & Reliability

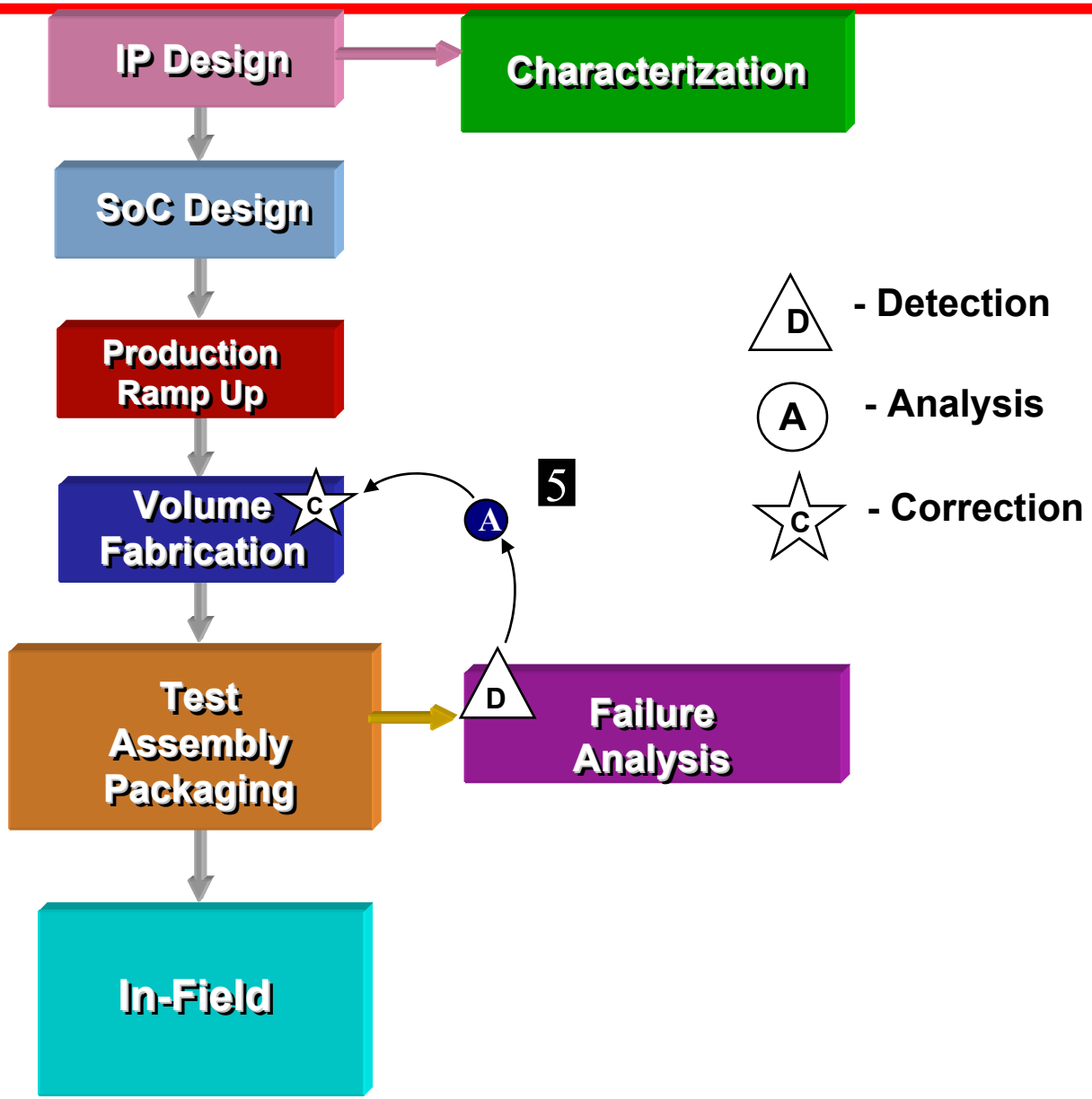
- Type and amount of redundancy
- Fault detection & location algorithm
- Redundancy allocation algorithm
- Repair Methodology
- Reconfiguration mechanism

2. Time-to-Market: Design

- Pre-Integrated F-IP and I-IP into a single SIP autonomous entity
- Interoperability
- Use of standard interface to I-IP, such as P1500



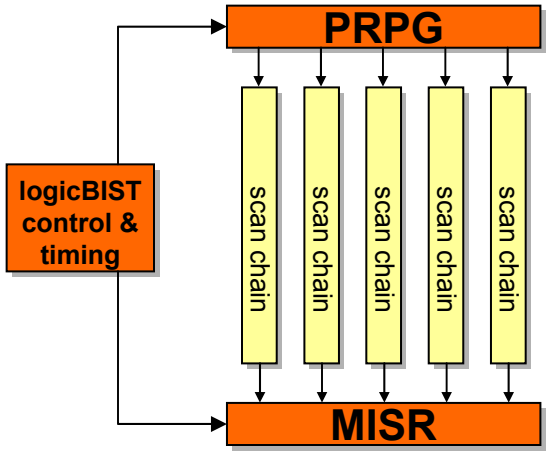
3. Embedded Diagnosis IP



3. Embedded Diagnosis IP

- Need to gather failure data using diagnosis IP and analyze obtained data by off-chip fault localization methodologies, tools and equipment
- Leverage same infrastructure IP for test, silicon debug and diagnosis
- Integrated Silicon Debug Solution comprised of -
  - Analysis & generate embedded test & diagnosis IP
  - Integration & simulation of embedded test & diagnosis IP
  - Creation of embedded test database
  - Failure data from diagnosis IP analyzed off-chip for fault localization

3. Infrastructure IP for Logic BIST



Pseudo-Random Pattern Generator

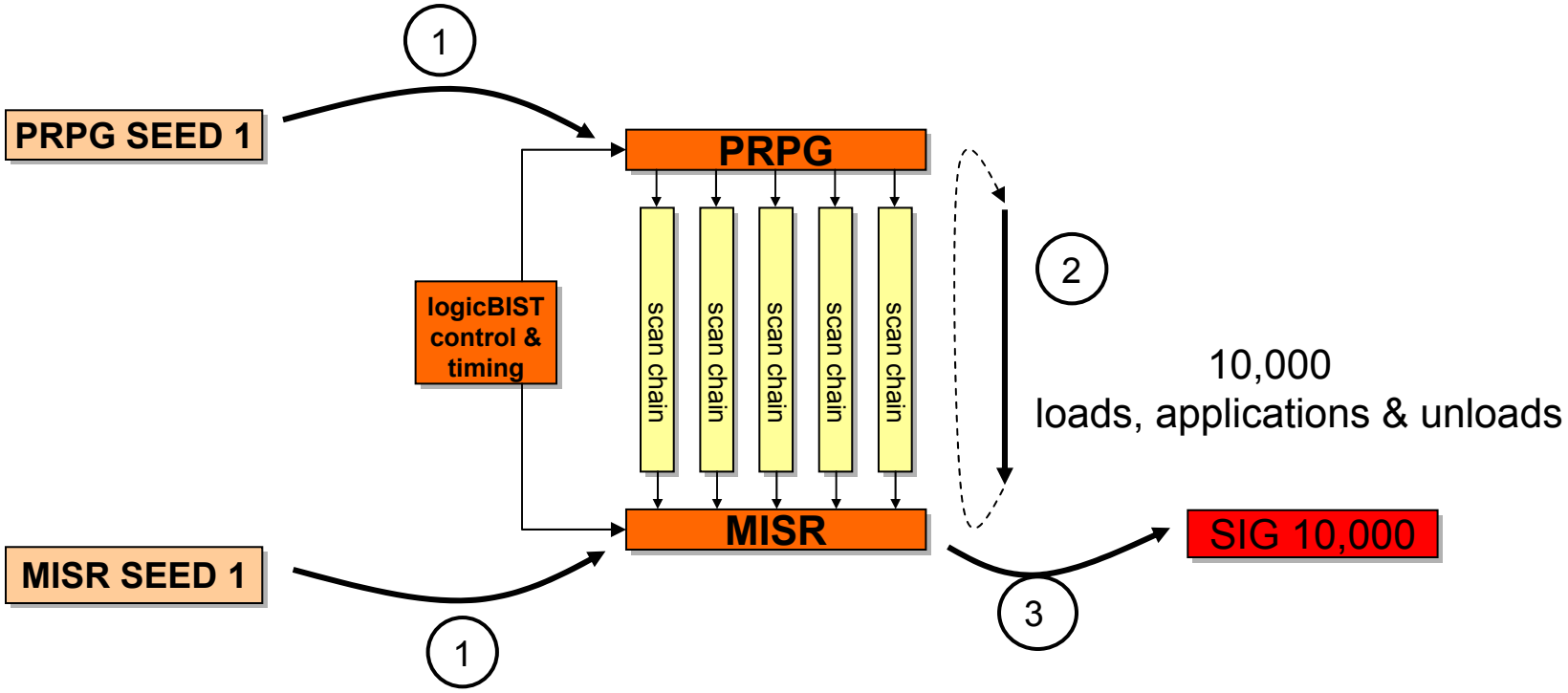
Control unit sequences all activity

All flops placed into large number of relatively short scan chains

Multiple Input Signature Register compresses responses into a signature

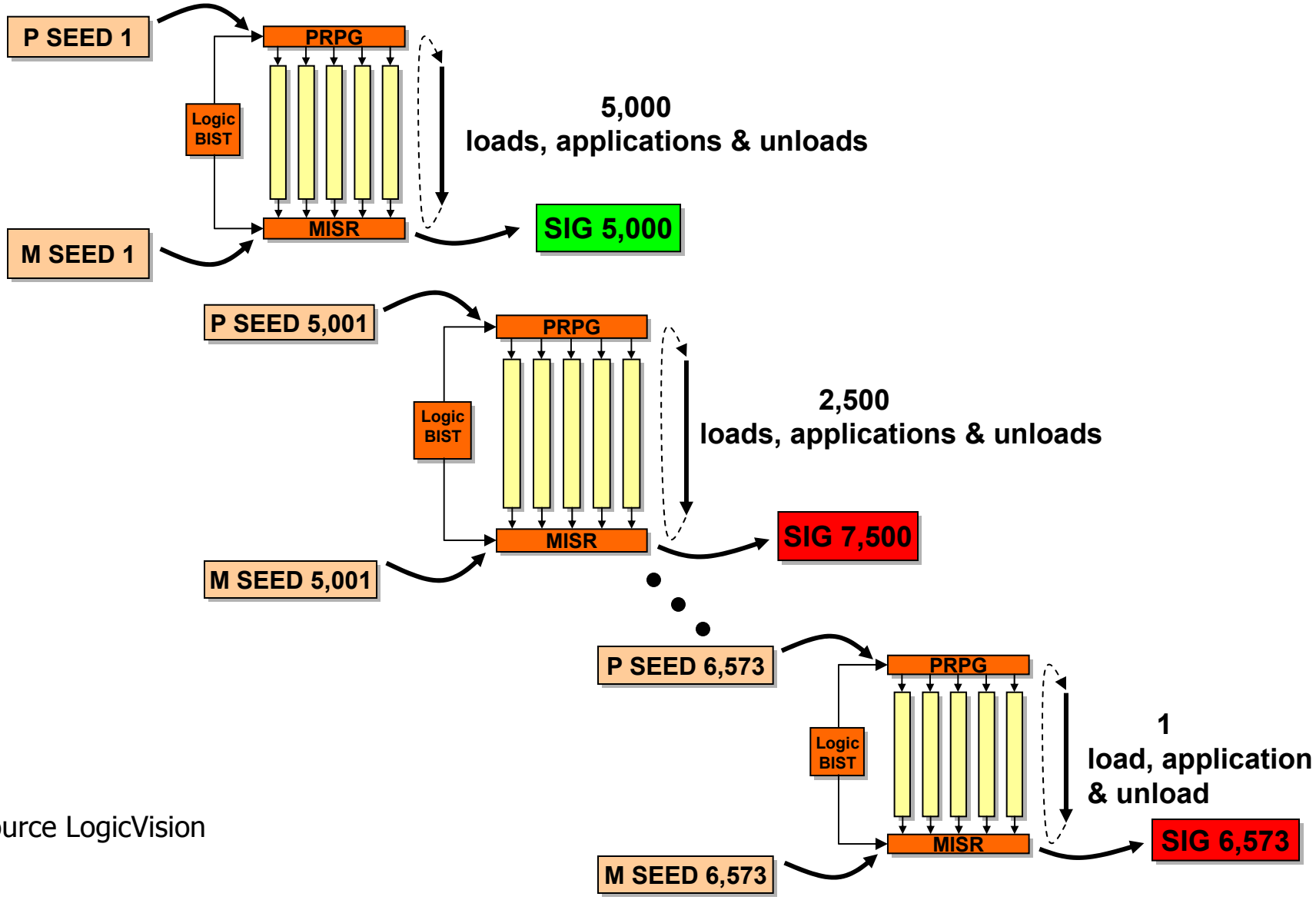
Source LogicVision

3. Logic BIST Test Sequence



Source LogicVision

3. Logic BIST Diagnosis- Binary Search



Source LogicVision

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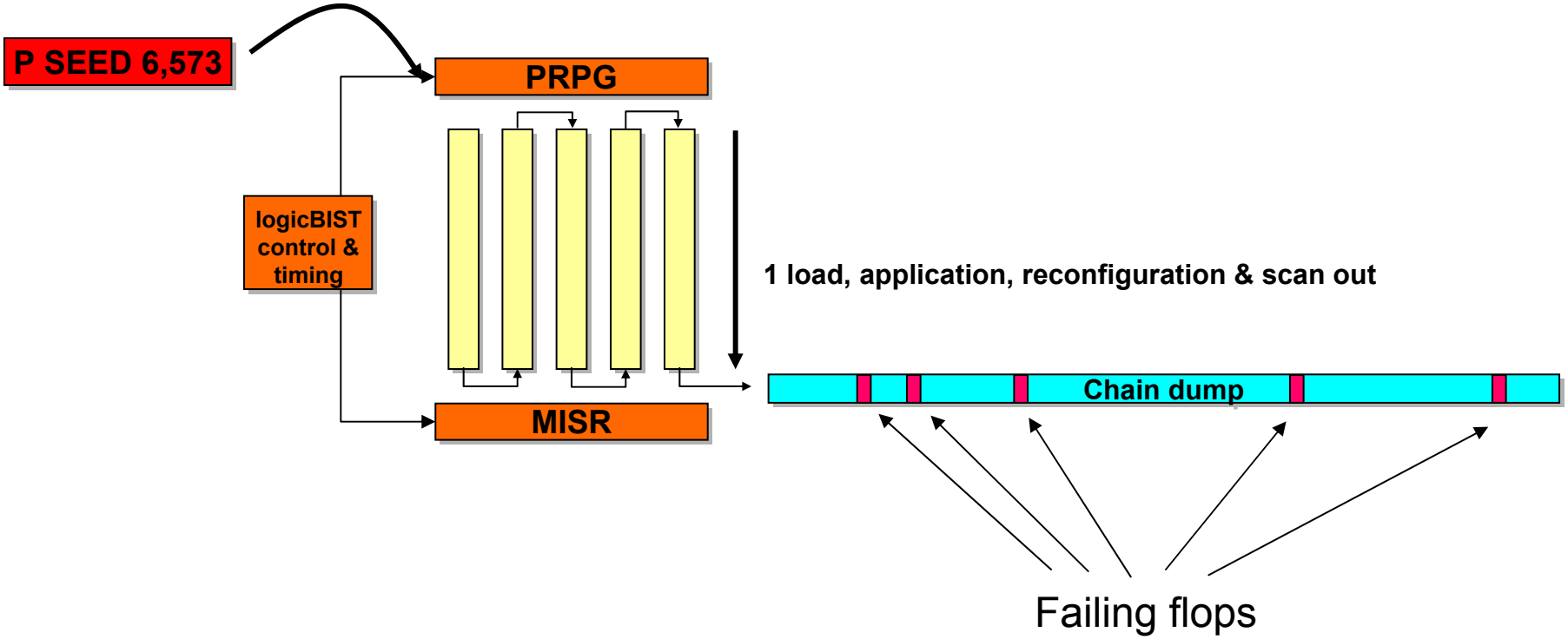
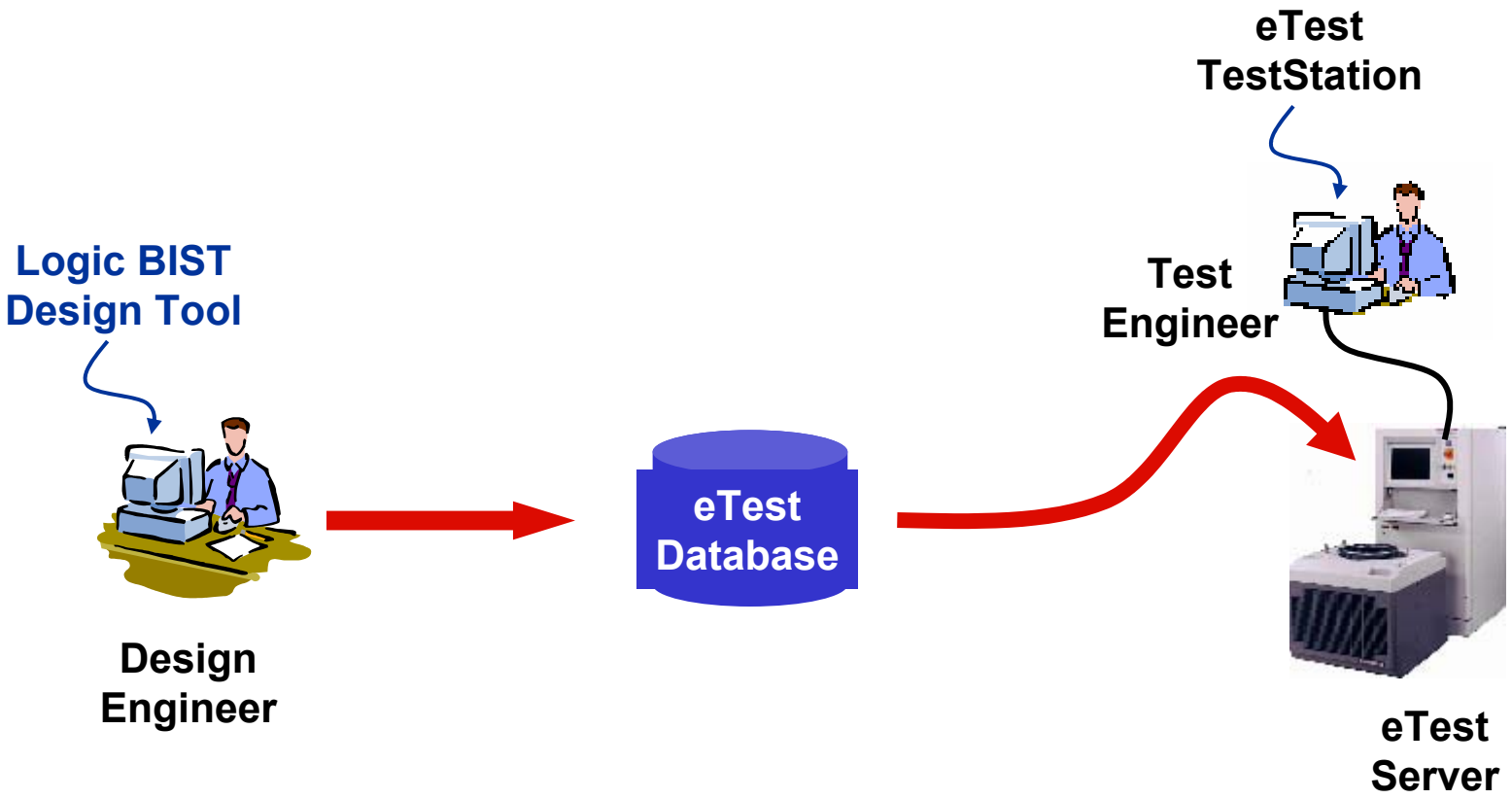


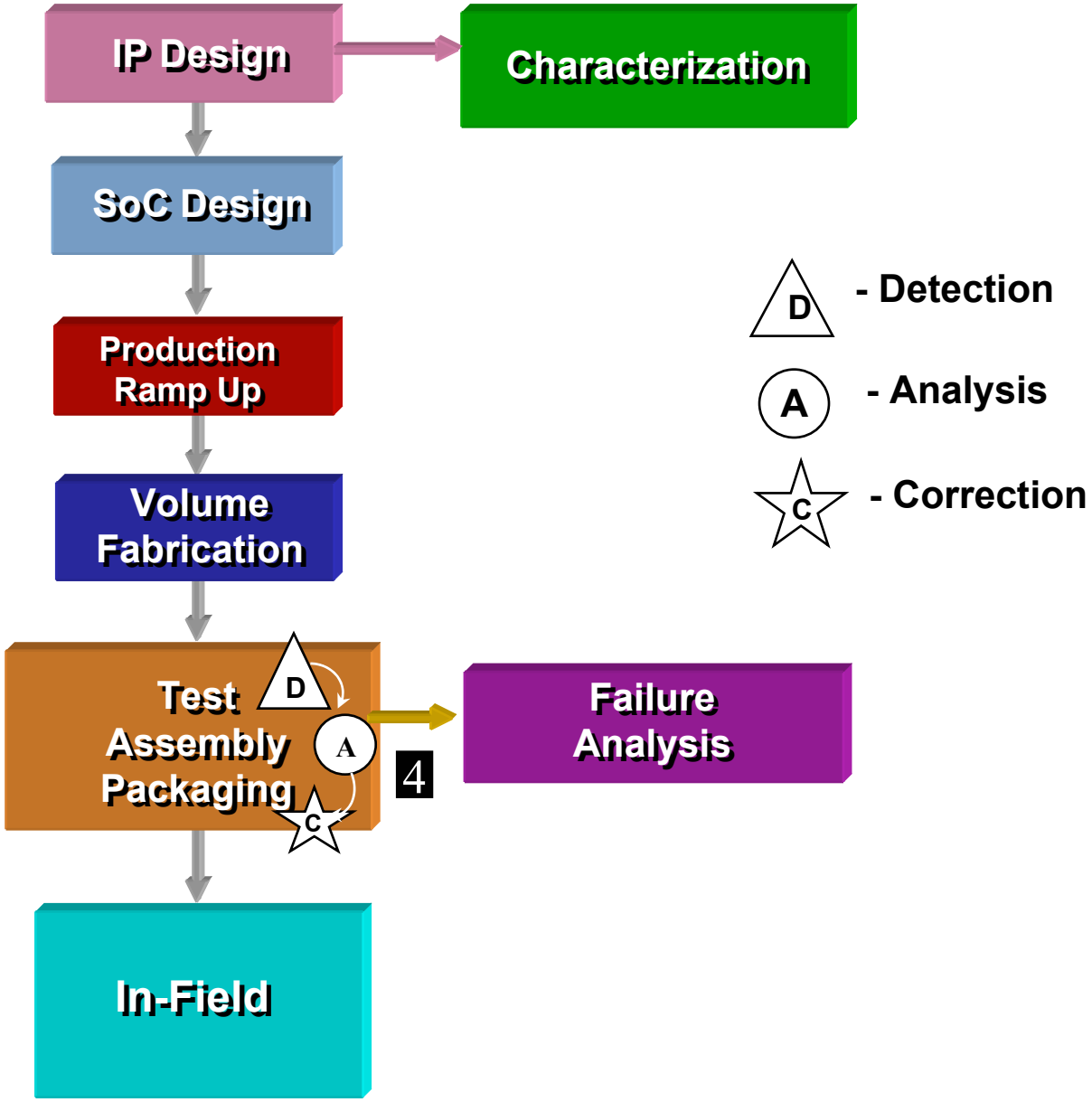
Source LogicVision

3. Integrated Diagnosis Solution



Source LogicVision

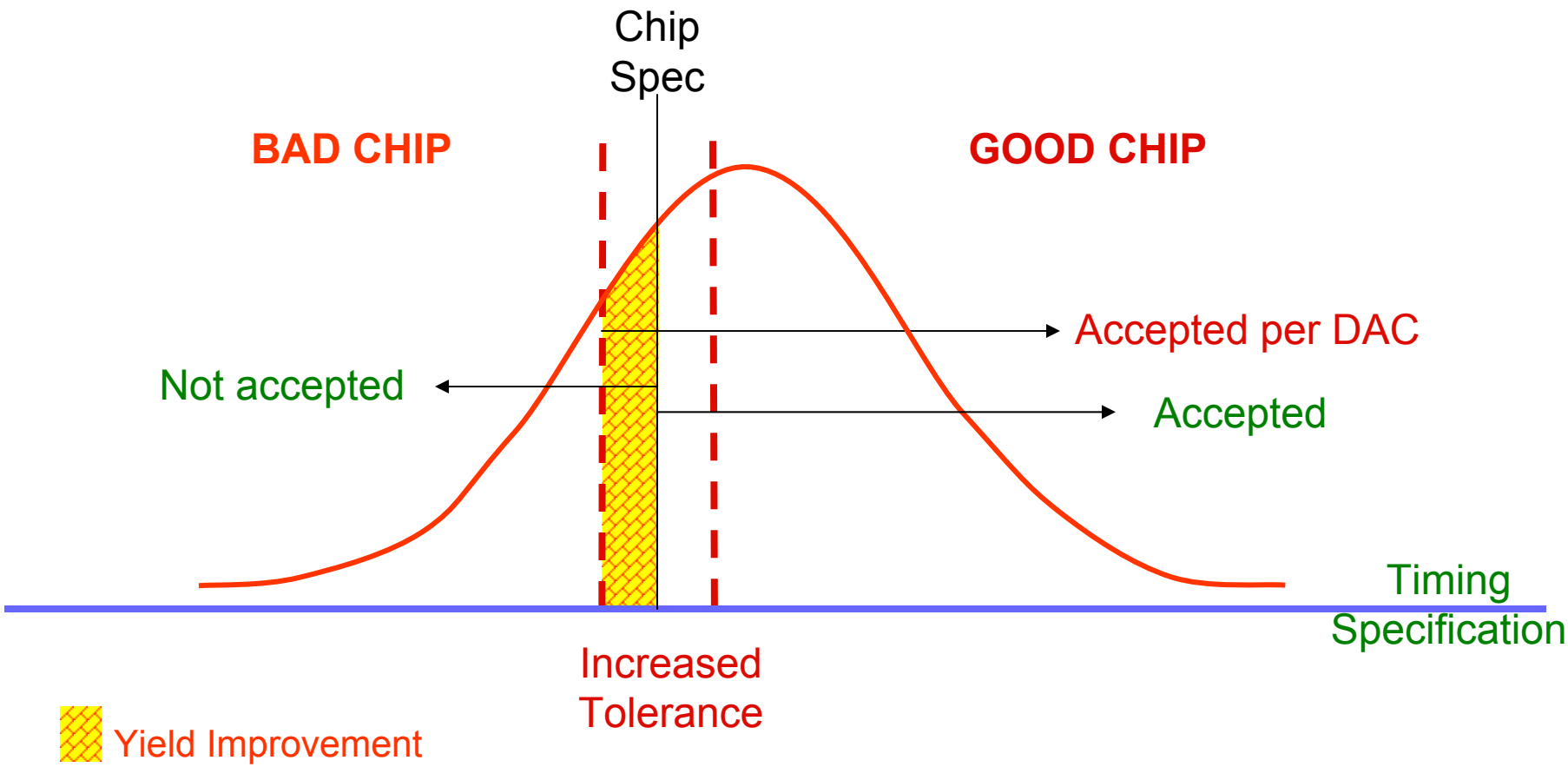
4. Embedded Timing IP



4. Embedded Timing IP

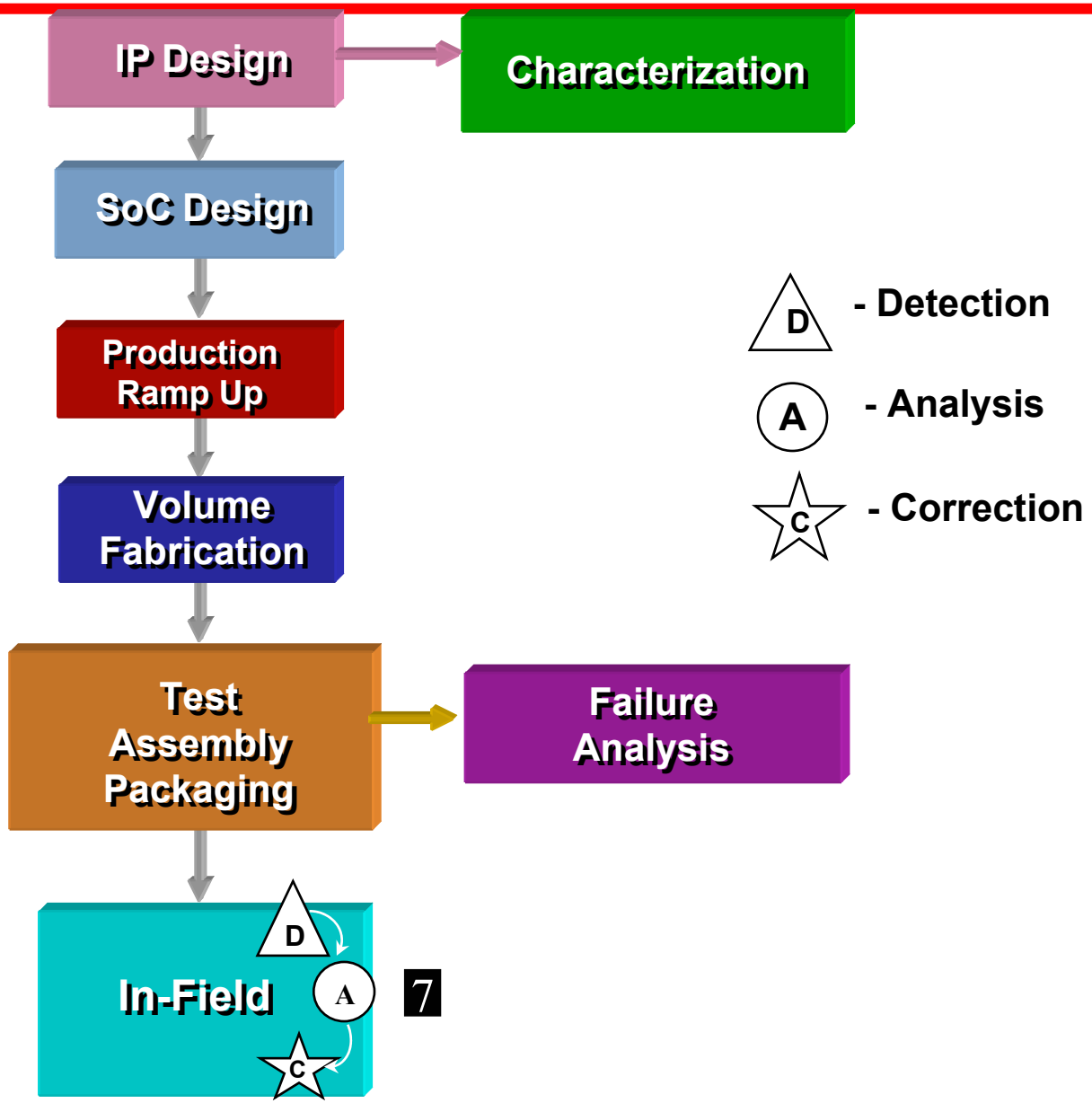
- Very stringent timing specification
- Difficulty in obtaining accurate measurements using external instrumentation
- Embedded timing IP [Tabatabaei 02] comprised of
  - Multiple high speed probes
  - Embedded control core directs probes and transfers information to timing processor for analysis
- Yield gain obtained due to accurate measurement

4. Yield Gain due to Timing IP

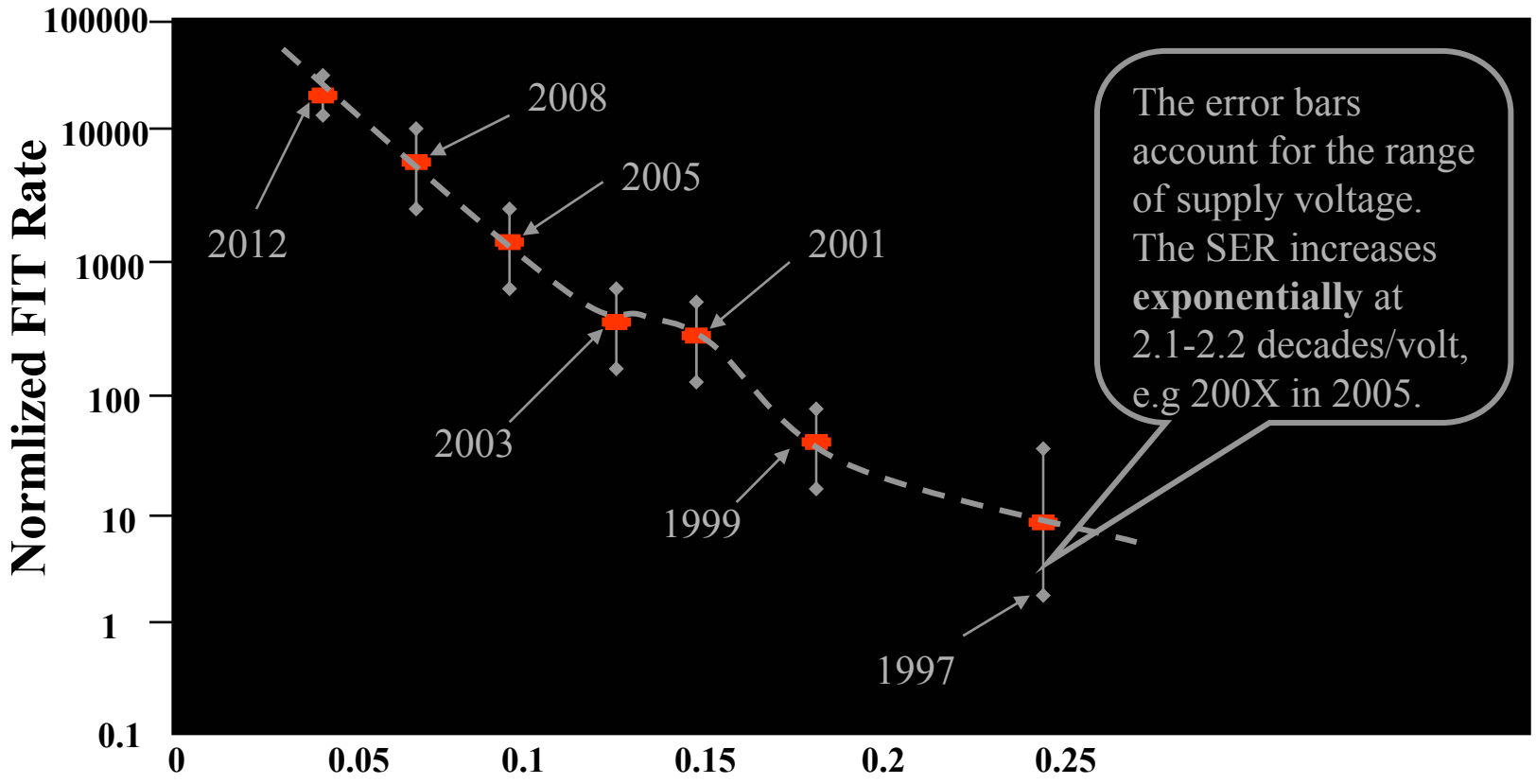


Source: Vector 12

5. Embedded Robustness IP



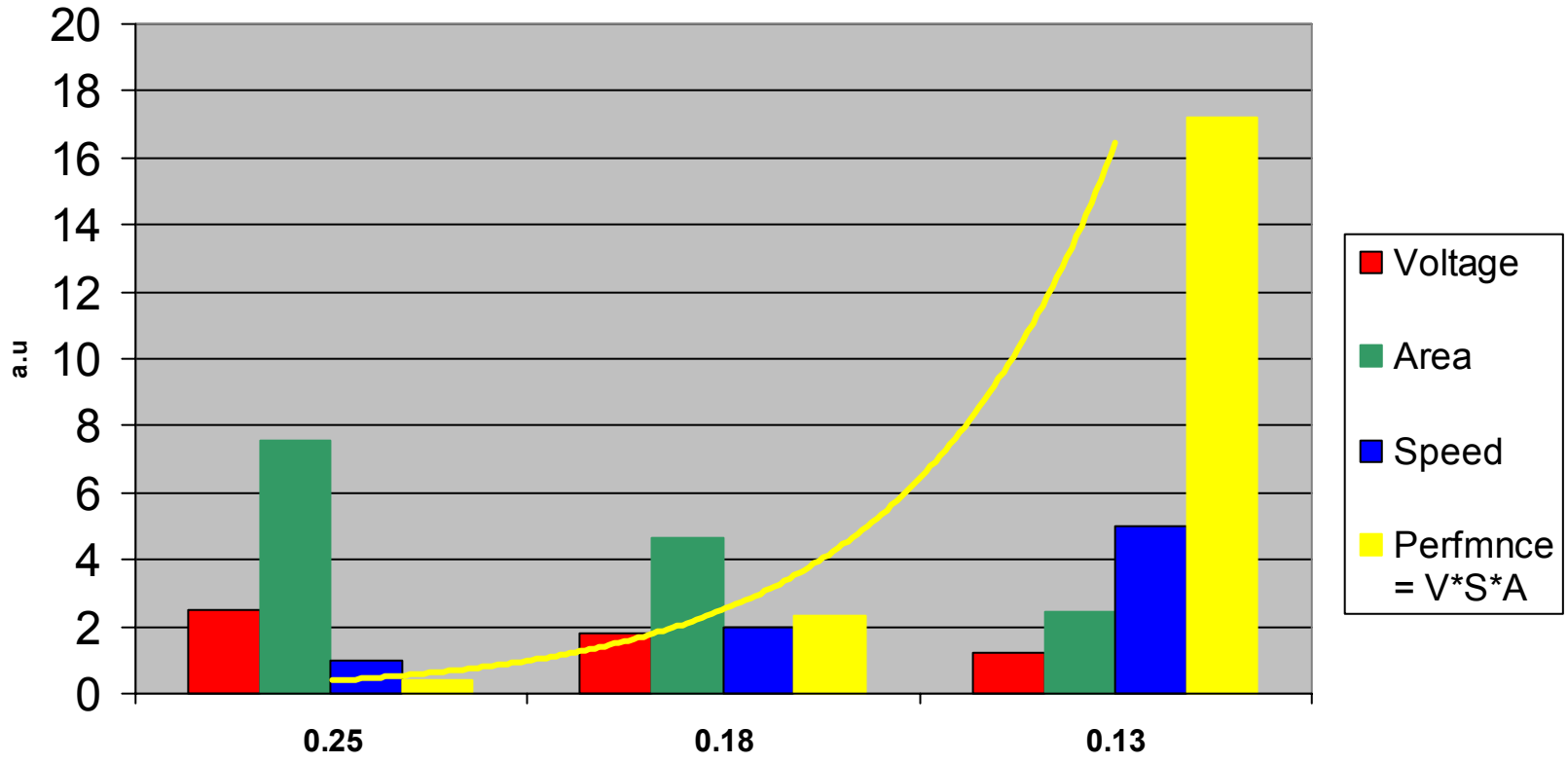
5. Field Reliability Challenge



From AMD, Intel, Compaq, 1999

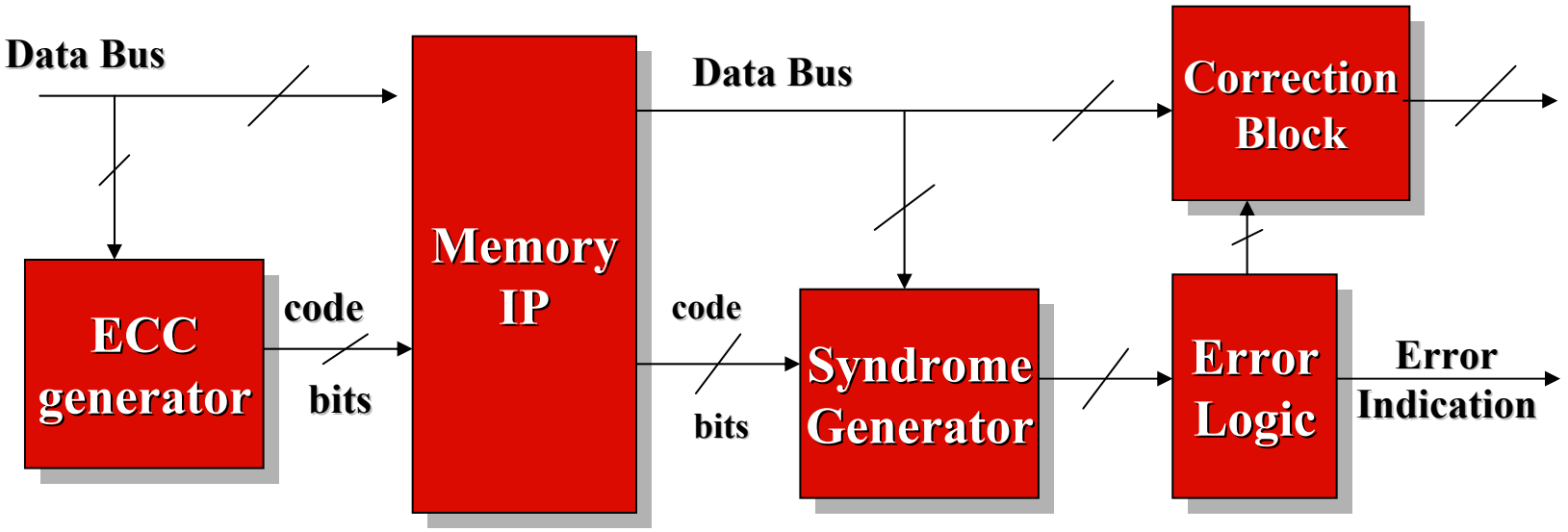
5. Soft Error Risk

- A 0.13µm design offers **40X** more performance than 0.25µm



… but is **40X** more prone to Soft Errors

5. Robustness IP for ECC



- Standard ECC architecture provides single bit repair and adds extra delay to each read and write operation

Conclusions

- Leveraging I-IP for higher yield and reliability
- Leveraging I-IP for Time-to-Volume Acceleration
- Infrastructure IP may require external support, automated tools and equipment
- Yield optimization loops leveraged at different product realization steps during design, fabrication, test and in-field
- Collaborative Environment is necessary to achieve Yield, Quality and TTV goals

THANK YOU FOR YOUR ATTENTION