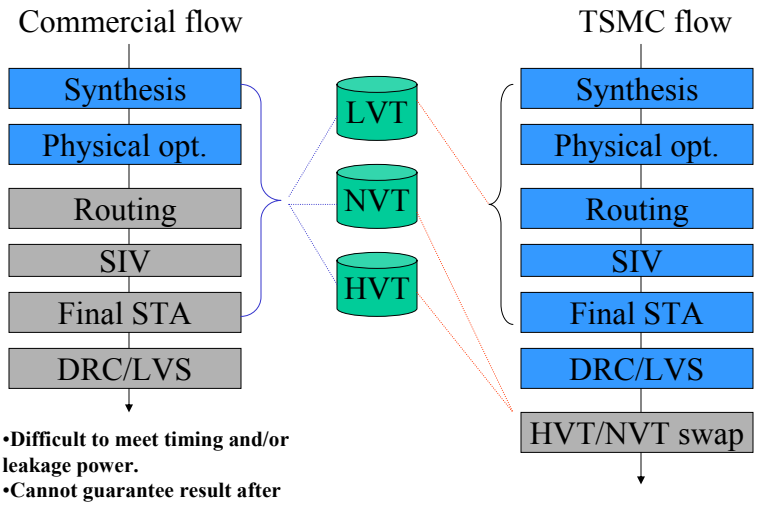
Design Challenges & Solutions for 90nm/130nm Technology

Contents

Design Flow to Minimize Leakage Power

- Leakage power and dynamic power are of the same order in 90nm technology.
- Multi-Vt core cell libraries can be used for performance and leakage power optimization.
- Use only the fastest library during all phases of flow to simplify handling and allow tool to fully optimize for timing and area
  - Difficult to achieve fastest timing if several libraries are used during synthesis and optimization.
- After final routing and placement, perform swapping of cells to NVT/HVT without causing new timing violations

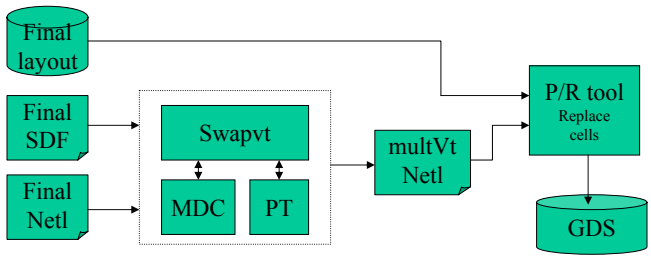
Design Flow to Minimize Leakage Power (Cont'd)



•Difficult to meet timing and/or leakage power.
•Cannot guarantee result after post-route iterations

Design Flow to Minimize Leakage Power (Cont'd)

- Advantages
  - No need to consider multiple libraries. Put all effort on optimizing area and timing
  - Simplifies implementation flow
  - Simple task to replace cells after final routing since it will not affect layout



Multi-Vt Flows Comparisons

2 DC iterations, long run time (5~10X longer)

	Lvt	Lvt -> Hvt --> 3vt (iteration 1)	Lvt -> Hvt --> 3vt (iteration 2)	Lvt swap Hvt/Nvt with our script
Leakage power (nW)				
before P&R	19.8	6.25	4.6	4.3
after P&R	19.8		6.9	4.3
Instance Count (%)				
Hvt		43%	44%	65%
Nvt		15%	23%	26%
Lvt	100%	42%	33%	9%
Timing (WNS)				
before P&R	0	0	0	0
after P&R	0		-0.4	0

A 90nm Test Case: ~100K cell instances with TSMC90 multi-vt libraries

Leakage and Performance Trade-off using Multi-Vt cells

A 90nm Risc Core

Vt options	Power (mW)		Frequency (mHz)	Cell distribution		
	Leakage	Dynamic		HVT	NVT	LVT
LVT	21.6	123.8	360			100%
LVT/NVT*	10.5	106.2	360		72%	28%
LVT/NVT/HVT*	9.7	105.5	360	43%	27%	28%
NVT	3.6	92.9	280		100%	
NVT/HVT*	2.2	91.5	280	73%	27%	
HVT	1.3	90.7	200	100%		

* TSMC Multi-Vt implementation approach was used

Note! No cells in paths with less than 0.3ns margin was swapped to NVT or HVT cells. If less margin is used, even more saving in leakage power can be achieved.

Signal Integrity Flows

- Xtalk
  - Prevention
  - Analysis
  - Violation fix
- De-coupling cell insertion
  - Capacitance calculation
  - De-coupling cell insertion

SI: Xtalk Prevention

- **Placement and optimization stage**
  - Set max transition (0.6 ~ 0.8 ns) to prevent weak victims
  - But sharp transition (0.4 ns) may create strong attackers
- **Post-placement stage**
  - FE: slew balance, congestion removal
  - Astro: gate up-sizing and buffer insertion for potential victims
- **Routing stage**
  - Nanoroute: global, track assign and detail route prevention
  - Astro route: global route and track assign prevention
- **Prevention effects**
  - Routing is more effective than placement in xtalk prevention
  - Can reduce xtalk violations 50% or more

SI: Xtalk Analysis

- Use CeltIc as our xtalk sign-off engine
- Library accuracy
- RC accuracy
- Design related information
  - Get timing window from PrimeTime
  - Identify constant nets and hazard-free net (spare cell nets, scan-in)
- Multi-Vt cells impact:
  - Xtalk sensitivity: HVt > StdVt > LVt

SI: Xtalk Fixing

- Flow 1: CeltIc -> FE -> Nanoroute -> CeltIc loops
  - Nanoroute is efficient in fixing glitch violations
  - FE is efficient in fixing timing violations
- Flow 2:CeltIc -> Astro-inroute -> CeltIc loops
  - Script for translating CeltIc violation report to scheme
  - Difference between CeltIc and Astro-xtalk:
    - Timing window, constant/floating nets, small cap filter
- Most Xtalk glitch and timing violation fixed in around 3 iterations.
- Manual script is used to fix remaining violations
  - High-strength victim nets (driven by D4 and larger cells)
    - wire spacing
    - buffer insertion
  - Low-strength victim nets (smaller than D4)
    - cell size up

Example Using Flow 1 (0.13u., 2M gates)

An example to show good noise convergence

	# of glitch violations	# of timing violations
Iteration 1	1437	622
Iteration 2	116	112
Iteration 3	18	40
Final Clean-up	0	0

De-coupling Cell Insertion

- De-coupling cap. cells are used to reduce dynamic IR drop on chip.
- C = P / f * V * △V
  - C: total decoupling cap
  - P: total power consumption
  - f: operating frequency
  - V: operating voltage
  - △V: voltage noise
- Decoupling cell cap =

  total decoupling cap – existing cap
- Existing cap sources:
  - Net cap, pin cap, power net cap
  - Internal pin cap, diffusion cap, nwell cap

Placement of Decoupling Cells

- Evenly distributed on power strap grids
  - Easy to implement and less effective on dynamic IR reduction
- Distributed based on power consumption
  - High power area
  - Clock buffers

DFM Scope and our Coverage

- DRM issues:
  1. Process variation modeling
  2. Metal over via/contact enclosure
  3. Redundant via insertion
  4. Dummy OD, Poly, and Metal insertion
  5. Poly/OD shape, orientation, dimension, and spacing
  6. Others

DFM: Interconnect Metal Process Variation Modeling

- Inter and intra-die process variation modeling
- Intra-die process modeling
  - Resistivity, metal width and thickness are function of width, spacing, and density.
  - Sample of resistivity, metal width and thickness adjustment table

	Width					
Spacing	0.20	0.40	0.60	1	2	3
0.21	2.653					
0.24	2.698					
0.42	2.339					
0.63	2.304					

S\W	0.20	0.40	0.60	1	2	3
0.21	0.389	0.389	0.389	0.389	0.389	0.389
0.24	0.389					
0.42	0.3					
0.63	0.3					
0.84	0.3					

S\W	0.20	0.40	0.60	1	2	3
0.21	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.24	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.42	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.63	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275
0.84	0.2275	0.4275	0.6275	1.0275	2.0275	3.0275

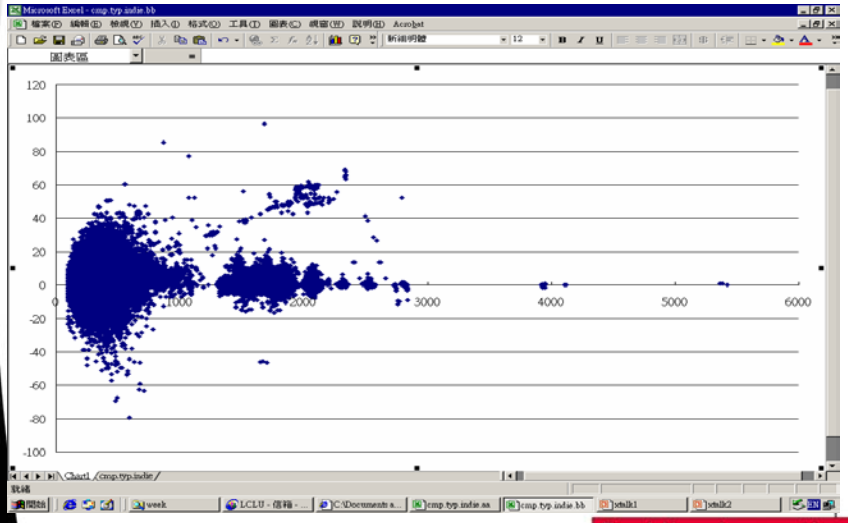
Resistivity

Thickness

width

Path Delay Comparisons of a 0.13um Example with and without Intra-die Metal Variation Modeling

x: path delay(ps), y: path delay diff (ps)



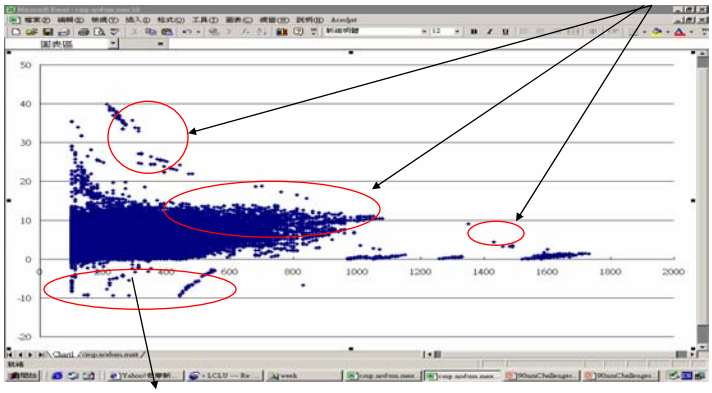
DFM: Inter-Die Metal Process Variation Modeling

- Process corners: too many combinations
  - Metal width (W), Metal Thickness, IMD thickness(IMD)
  - Which ones ?
    - **Cmax**(Wmax, Tmax, IMDmin), **Cmin**(Wmin, Tmin, IMDmax)
    - **RCmax**(Wmin, Tmin, IMDmin), **RCmin**(Wmax, Tmax, IMDmax)
  - Are all metal layers varied to the same corner?
- Current work-around for interconnect corner modeling:
  - Use extra margin for interconnect R and C
  - Use RC max/min corners
  - Use RC max/min and Cmax/min corners

A 90nm Example to Show Metal Process Corner Impact on Path Delay (Cmax corner vs. Typical)

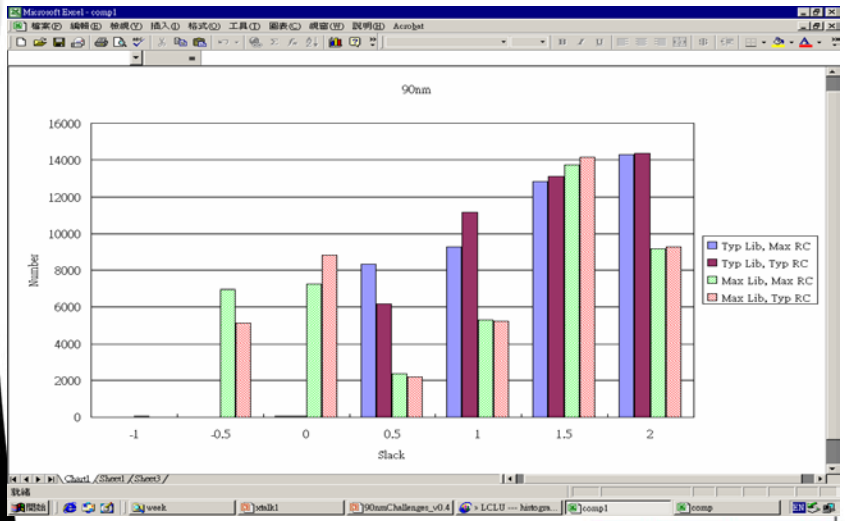
x: path delay(ps), y: path delay diff (%)

Design Margin if typ. Corner is used

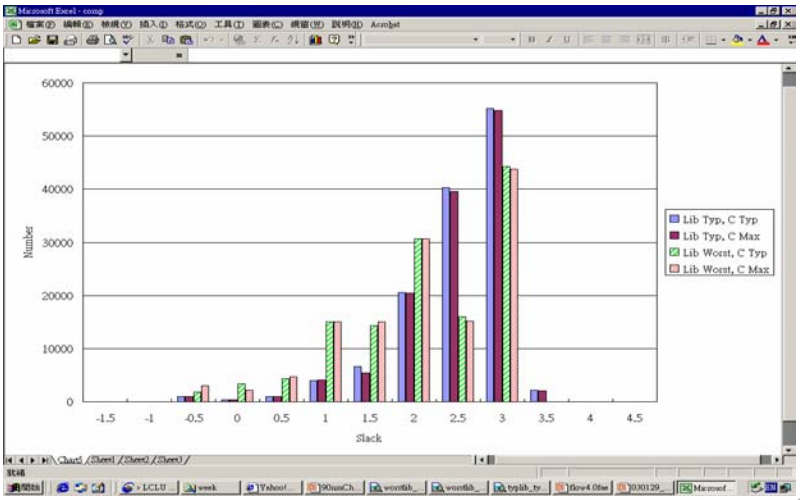


Extractor's accuracy limitation

Delay Impact Comparisons of library and Interconnect corners: A 90nm Example



Delay Impact Comparisons of library and Interconnect corners: An 130nm Example



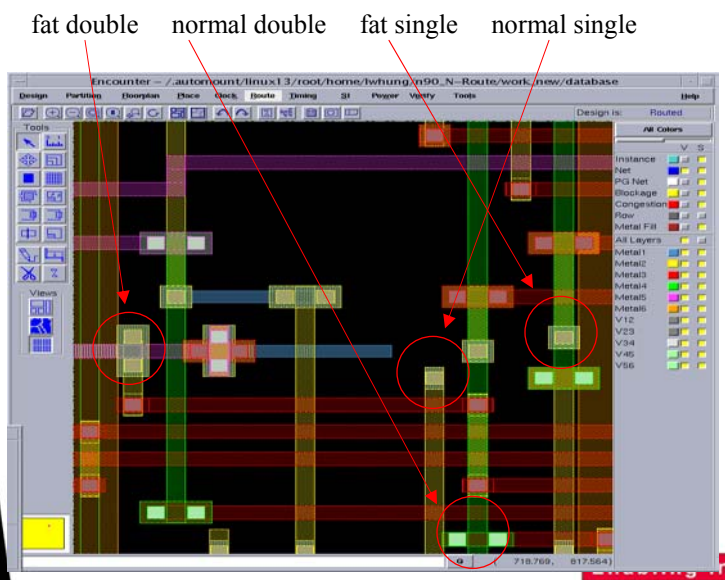
DFM: Redundant Via Insertion methodology

- In addition to add double vias on wide metal, suggest add redundant vias on normal signal for yield improvement.
  - Both Astro and Nanoroute support this feature now and are used in our 90nm projects.
- A 4-stage redundant via insertion flow:
  - fat double via > normal double via > fat single via > normal single via

DFM: Redundant Via Insertion methodology (Cont'd)

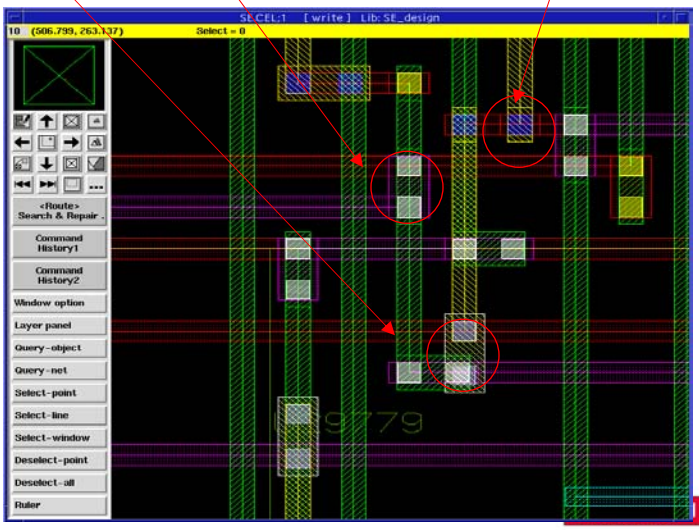
- Redundant via insertion flow:
  - Define 4 via types in P&R tech. files
  - Step 1: route with single via
    Fat single via first if DRC OK
    Then, normal single via
  - Step 2: swap single via to double via
    Fat double via first if DRC OK
    Then, normal double via

DFM: Double Via Insertion in Nanoroute



DFM: Double Via Insertion in Astro

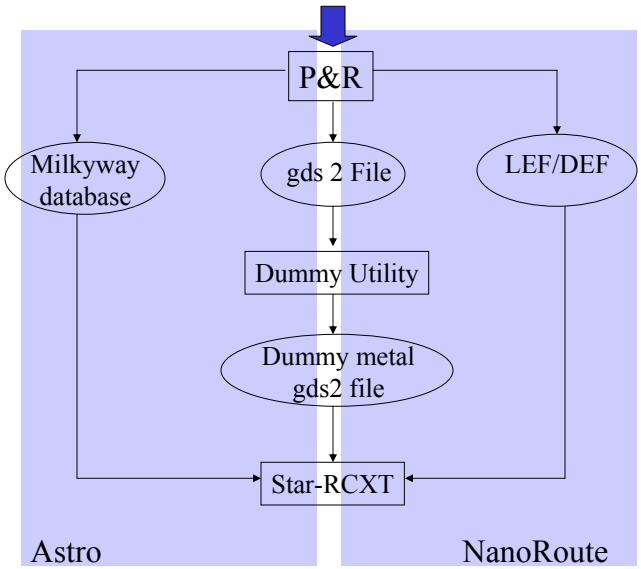
fat double normal double no fat single normal single



DFM: Dummy Metal Insertion

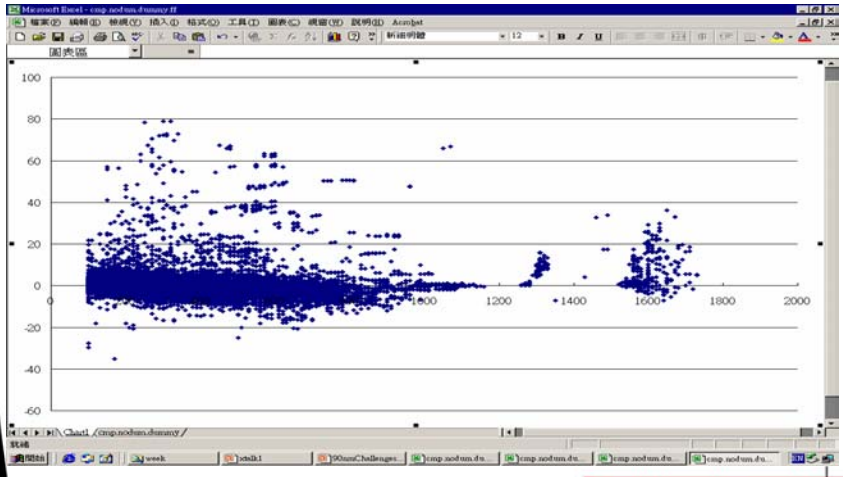
- Dummy pattern selection: size and spacing
  - must meet metal density requirement
  - minimize OPC impact
  - minimize induced capacitance
- Dummy metal flow:
  - Insertion of dummy metal
  - Induced delay analysis
  - Final DRC check
- Add dummy metal as a post-processing step
- Dummy metal induced capacitance can be extracted and verified in final timing check.

DFM: Dummy Metal Insertion Flow



A 90nm Example of Dummy Metal Impact on Delay

x: path delay(ps), y: path delay diff (ps)

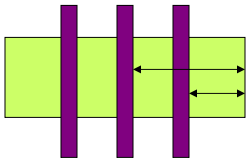


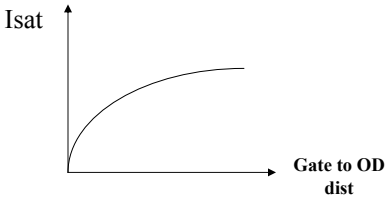
DFM Analyzer

- Cont/Via enclosure by metal.
- Poly corner rounding effect (“T’ shape).
- OD corner rounding effect.
- Cont. position and number affects Idsat.
- OD resistor increasing while gate is too close.

LOD Effect Modeling

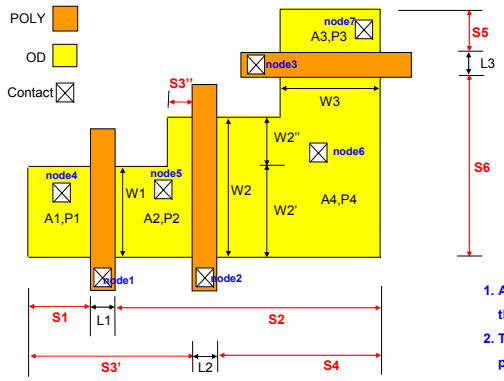
- Gate to diffusion edge distance must be extracted to model STI stress effect in design.
  - Spice model: available for early user now
  - Extractor: available now in Hercules/Star-rctx and Calibre/xCalibre flows





I_{sat} is a function of gate to OD edge spacing.

LOD Effect Modeling (Cont'd)



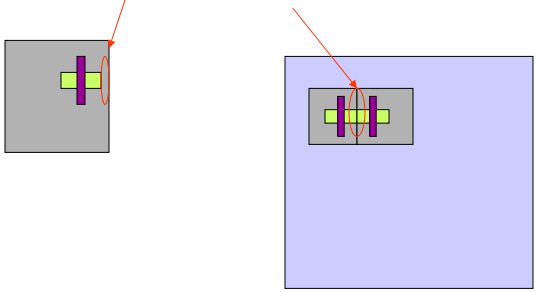
1. Add more instance parameters in the device.
2. The number of additional instance parameters is not a constant and is dependent on the shape of layouts.

Extracted Netlist of The Above Layout:

M1 4 1 5 0 n_ch L=L1 W=W1 AD=A1 PD=P1 AS=A2/2 PS=P2/2 SA=S1 SB=S2
M3 6 3 7 0 n_ch L=L3 W=W3 AD=A4/2 PD=P4/2 AS=A3 PS=P3 SA=S6 SB=S5
M2 5 2 6 0 n_ch L=L2 W=W2 AD=A2/2 PD=P2/2 AS=A4/2 PS=P4/2 SA=S3' SB=S4 SW=W2' SA=S3'' SB=S4 SW=W2''

LOD Effect Modeling (Cont'd)

- IP design
  - Reserve space margin from OD to cell boundary to avoid OD abutment in chip placement.
- Chip integration
  - Make sure no OD abutment after cell placement.



TSMC Reference Flow 4.0

- Previously presented design solutions for noise, dynamic IR, DFM, and leakage power optimization flows will be integrated in TSMC Reference Flow 4.0
- Available on TSMC ONLINE in early May 2003.
- Several 90nm and 130nm chips were taped out using TSMC Reference Flow 4.0 + TSMC 90nm/130nm core cell libraries.
- Working on high frequency CTS design, flip chip area array flow, voltage island methodology now.

TSMC Reference Flow 4.0 Diagram