Layout Methodology Impact of Resolution Enhancement Techniques

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ABSTRACT
This paper introduces resolution enhancement techniques (RET), discusses the impact that RET have on the physical design and chip layout flow, and proposes two alternative future methodologies.

Keywords
Lithography, resolution enhancement techniques, design for manufacturability, radically restricted designs.

1. INTRODUCTION
While optical lithography has been a key enabler to rapid integration in the microelectronics industry, resolution demands have outpaced the introduction of advanced lithography hardware solutions and made lithographic patterning increasingly difficult. As a result, increasingly complex resolution enhancement techniques (RET) have been required to maintain adequate pattern fidelity. As optical lithography is being pushed closer to its fundamental resolution limit, it is becoming increasingly difficult to implement RET without RET-enabling layout restrictions. While the impact of these restrictions on design rule checking and layout density has been discussed previously (DAC reference), this paper focuses on the impact of RET-enabling layout restrictions on established design methodologies.

2. FUNDAMENTALS OF OPTICAL LITHOGRAPHY
2.1 Conventional Resolution Limits and Enablers
The resolution limit of a conventional optical lithography system with on-axis illumination can be approximated as

$$R_{min} = 0.5\ \lambda/NA \quad (1)$$

where λ is an illumination wavelength, NA is a numerical aperture, and R_{min} is the minimum feature size, or half the smallest resolvable feature pitch. This equation assumes coherent imaging and a binary system (i.e. using non-phase shifted photomask). How close any given lithography process comes to this theoretical resolution limit is commonly expressed by the Rayleigh factor k_1,

$$R_{min} = k_1\ \lambda/NA \quad (4)$$

Under these assumptions, resolution is proportional to λ and inversely proportional to NA, thereby offering two physical quantities for the reduction of printable half pitch. Unfortunately, it is difficult to increase resolution by increasing NA, because the second fundamental lithography parameter, the depth of focus (DOF, the range of defocus over which adequate feature fidelity can be maintained) has an inverse square dependency on NA:

$$DOF = \lambda/(2NA^2) \quad (5).$$

The Rayleigh factor is also often used as a unit less measure in lieu of feature size, as it expresses how difficult it is to resolve a certain dimension with a given lithography tool:

$$k_1 = \text{Dimension}\ (NA/\lambda) \quad (5)$$

Table 1 shows how lithography solutions have evolved as smaller features sizes are demanded. As expected, wavelength has been decreasing and NA has been increasing. However, k_1 has been continuously declining spite of tooling improvements, i.e., lithography has been loosing ground due to ever harder technology generations. Finally, for each technology generation two distinct lithography solutions can be identified, a very aggressive, low k_1 development phase followed by a somewhat relaxed manufacturing phase.

Node	Year	Min pitch	Developm. λ/NA	Manuf. λ/NA	Develop m. k1	Manuf. k1
180	1999	500	248 / .5	248 / .75	.5	.76
130	2001	300	248/ .75	193 / .75	.45	.58
90	2003	214	193/ .75	193 / .85	.42	.48
65	2005	160	193/ .85	(157/.9)	.35	(.45)
45	2007	130	(157/.9)	?	(.37) .3	?

Table 1. λ/NA solutions for technology nodes and erosion of k_1

2.2 Resolution Enhancement Techniques
As the k_1 factor started to dip below 0.5 resolution enhancement techniques (RET) had to be applied to restore image fidelity. Two examples of RET that enable manufacturing lithography at or slightly below k1=0.5 are attenuated phase shifted masks (attPSM) and optical proximity correction (OPC).

2.2.1 Attenuated Phase Shifted Mask Lithography
AttPSM lithography improves pattern fidelity by 'darkening' the edges of shapes through destructive interference of light using a mildly translucent photomask. Now commonly called 'embedded attenuated phase masks', mask substrates are used that allow a small amount of light (6-10%) to penetrate the normally opaque mask regions. Through careful material optimization, the background light penetrates the mask exactly 180° out-of-phase with the light penetrating the clear regions of the mask. As illustrated in Figure 1, this phase shifted background light improves feature contrast at the edges of the printed image. Forcing the electric field vector of the background light to be negative by shifting it 180° relative to the foreground light causes a dark rim in the intensity profile. This 'crisping up' of the printed images helps to recover some patterning fidelity, but it does not fundamentally improve the resolution or DOF as outlined in Equations 3 and 8. Note that, since attPSM results in no inter-

shape phase interference, it can be applied to arbitrary layout configurations with no design restrictions.

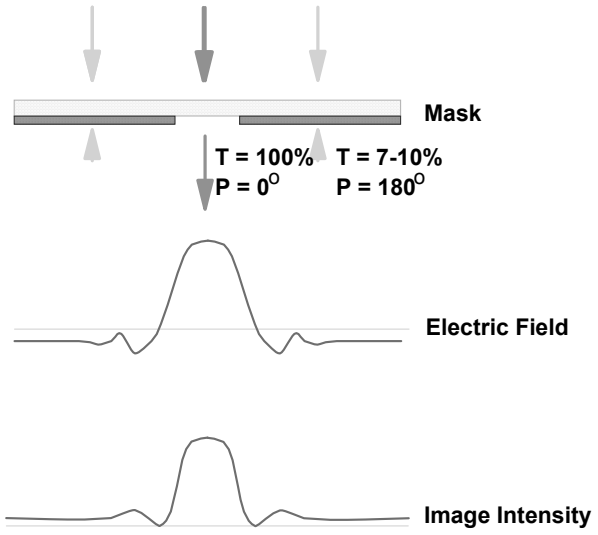

Figure 1, Principle of attenuated phase shifted mask (attPSM)

2.2.2 Optical Proximity Correction

Schematically outlined in Figure 2, OPC begins by characterizing the patterning operation and all its inaccuracies from various sources such as mask build, wafer exposure, etch, etc. In the now commonplace 'model-based OPC' this mathematical description of the process is used in iterative optimization routines to pre-distort the mask shapes to compensate for known, systematic, and modeled patterning inaccuracies.

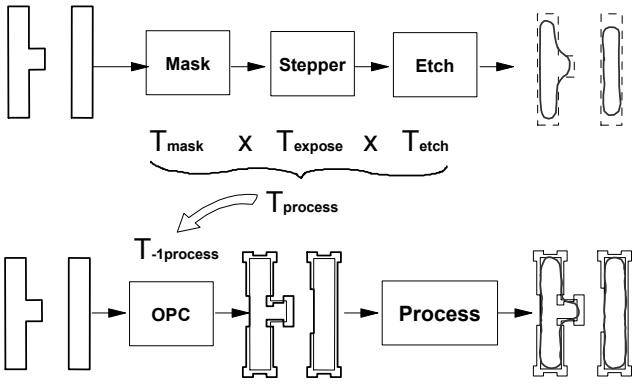

Figure 2, Optical proximity correction

OPC improves the 'effective resolution' of a patterning process by overlapping the conditions with which different feature types can be imaged accurately. Nested features typically image on-size and with the best image quality at a different exposure dose than isolated features. Biasing the mask patterns appropriately will allow both feature types to be imaged adequately in a single exposure. However, OPC does not change the fundamental resolution limits of a lithography system.

2.2.3 Layout Methodology Implications of RET

All the RET implemented up to the 90nm technology node have not altered the fundamental layout methodology as shown in Figure 3. Layouts are generated based on design rules that are enforced through design rule checking (DRC). In this flow, the escalating lithography difficulty is acknowledged through increasingly invasive layout restrictions, but the fundamental layout methodology remains intact.

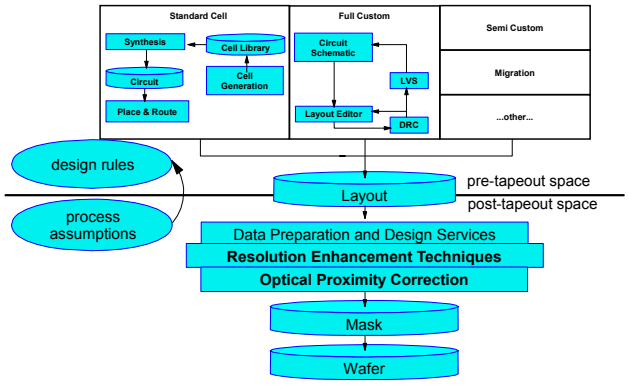

Figure 3, diagram of conventional, DRC-enabled layout flow

3. Future Technology Nodes

3.1 Hardware Options

As shown in Table 1, the 65nm technology node (often referred to as the 1st sub-100nm technology node) is using high-NA 193nm lithography at an extremely small k_1 of about 0.35 in development. Ultra-high NA 157nm lithography is the upfront choice of manufacturing lithography for the 2005 technology node, as it would provide some relief of this extremely difficult resolution challenge but would still leave the k_1 well below 0.5. Unfortunately, technical challenges, predominately related to optical material issues, coupled with significant economic challenges, have caused the 157nm lithography program to slip behind schedule [2]. As a result, 157nm lithography will be late for the entire 65nm technology node, since an integrated 157nm process will probably not be ready for manufacturing until 2007.

The prospect of lowering the illumination wavelength to 13.5nm makes Extreme Ultra Violet (EUV) lithography a very attractive proposal. Illuminating a reflective reticle, manufactured by stacking 40-50 Mo/Si bilayers at atomic-scale accuracy, with light emitted by a laser produced plasma which is formed by zapping a Xenon medium with a high power laser in vacuum at very low power conversion efficiency, puts EUV in the technical challenge ballpark of the ICBM defense star-wars initiative. In spite of its technical complexity, EUV is currently moving out of the national laboratories into early commercialization [3]. However, it is unrealistic to assume that EUV will have any impact on either the 65nm or 45nm nodes.

Since a shorter illumination wavelength is not available, immersion lithography uses a well-known microscopy trick to improve resolution. Adding a higher index of refraction material in the gap between the pupil and the wafer can improve lithographic resolution, because the resolution of the system is defined on the wafer side of the projection lens and the resolution and DOF should more correctly refer to the wavelength of the exposure light in the medium filling the gap. Immersion lithography is challenging, as it requires introducing wafers in a cleanroom into a watery or oily substance, scanning a precision

lens in close proximity at very high speeds, and removing the wafers for further processing. Despite recent discussions on this technique [4], it is hard to even estimate availability dates.

3.2 Strong-RET

Since, hardware solutions will be insufficient for 65nm technologies, how can chips be manufactured at $k_1 = 0.35$ if the fundamental limit of conventional lithography is $k_1 = 0.5$? Strong RET provides a solution based on 2-beam imaging. If one of the light sources approximating the mask openings is 'pushed back' by ½ λ, a very different diffraction pattern is obtained. Since the first interference now occurs at an angle that adds ½ λ pathlength difference (rather than 1 λ for conventional lithography) the minimum set of diffracted orders required to form an image for a given pitch are much closer to the center of the imaging lens. For a given NA, the ultimate half-pitch resolution is now given by

$$R_{min} = 0.25\ \lambda/NA \quad (11)$$

or a $k_1 = 0.25$. In addition, no constructive interference occurs at the 0^o angle (the light sources are ½ λ out of phase), so the perpendicular beam is eliminated and with it the DOF limitations of Equation 9. Therefore, 2-beam imaging provides 50% resolution improvement and significantly enhanced DOF.

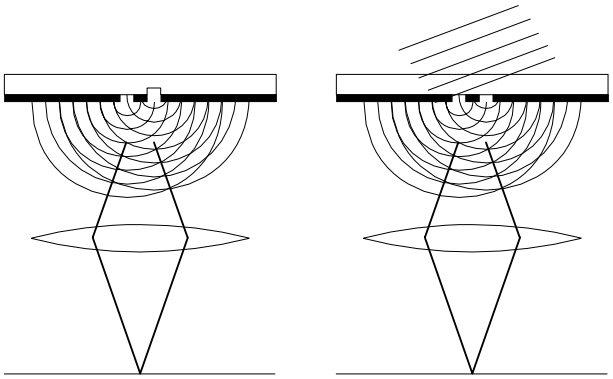

Figure 4, altPSM (left) and OAI (right) produce 2-beam imaging

Two means of achieving 2-beam imaging are shown in Figure 4. To obtain the ½λ phase offset, alternating phase shifted mask lithography (altPSM) manipulates the mask topography to recess juxtaposed mask openings by

$$\text{Etch Depth} = 0.5\ \lambda / (n-1) \quad (12)$$

where n is the refractive index of the mask substrate, typically around 1.4. Off-axis illumination (OAI) achieves the same effect by illuminating the mask at the appropriate angle

$$\sin\theta = 0.5\ \lambda / \text{Pitch} \quad (13)$$

More details on these strong-RET techniques are provided next.

3.3 AltPSM challenges

AltPSM is illustrated in Figure 5 on a pair of transistor-like structures. The resolution-enhancing phase shift is created across the narrow portion of the opaque mask structure, with juxtaposed mask regions exhibiting a step height difference. As shown in the cross-section right of the layout, this is achieved by recessing the appropriate mask region. This causes the electric field amplitude of the imaging light to reverse sign and yields high contrast shadows for the narrow images.

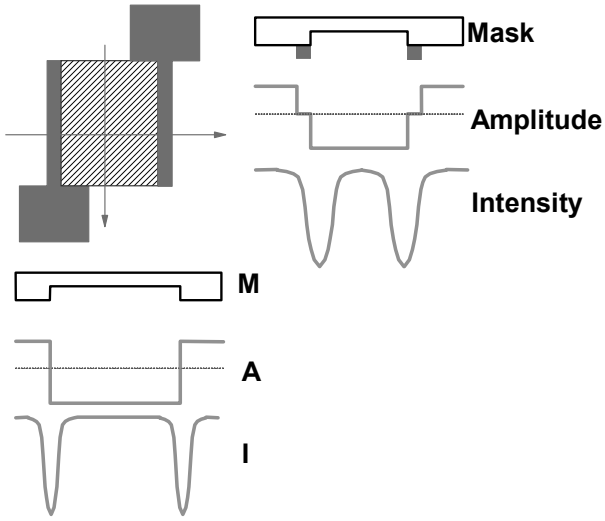

Figure 5 Principle of altPSM

Unfortunately, the recessed region of the mask cannot always terminate on opaque features, causing the printing of unwanted residual images along the phase step as shown in the cross-section below the layout. To address this problem, the lithography community has proposed a double exposure process, as shown in Figure 6. In this dark field alternating process the narrow layout segments are imaged by the phase shifted mask (left, layout and image) and a second exposure is used to remove residual images and fill-in the wider portions of the layout (right). The two images add in the photo resist to reconstruct the original pattern (bottom). While this process adds manufacturing cost, it does not result in additional design impact.

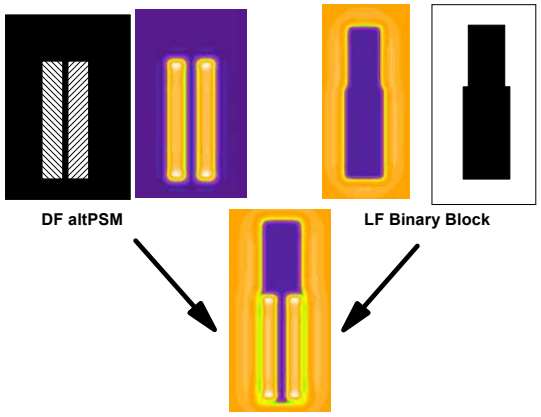

Figure 6 Double exposure altPSM

Identifying mask regions to be recessed requires adding phase shapes to the layout. Lithography and mask manufacturability dictate shape dimensional constraints which in turn prohibit the addition of legal phase shapes to arbitrary layout configurations, driving the need for altPSM-enabling layout restrictions. Layout configurations that are otherwise design rule clean can lead to 'uncolorable' phase errors. A small hypothetical layout (original pattern in solid black, regions of opposite phase in diagonal-

hatch) that violates no intra- or inter-shape design rules, yet causes an un-resolvable phase conflict, is shown at the top of Figure 7. Multiple solutions to the phase conflict are also shown. The optimum layout solution will depend on the specific layout objectives. Key challenges in the implementation of altPSM are (1) lack of reliable design rule checking to guarantee phase-compliant layouts [5] and (2) difficulty in converting abstract colorability feedback into required layout modifications.

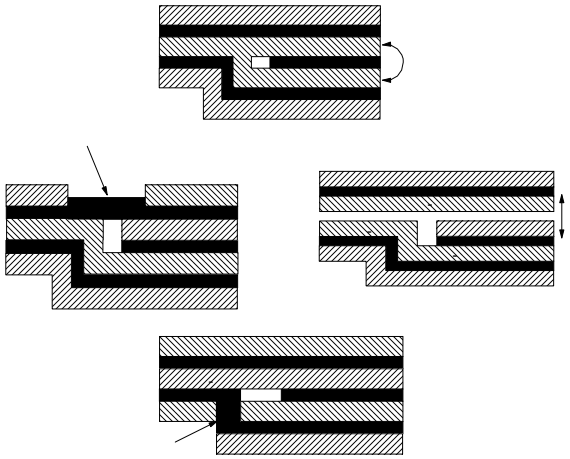

Figure 7 Sample layout conflict (top) and possible solutions

3.4 OAI Challenges

In OAI, the image is formed by interference between a light beam transmitted perpendicular through the mask (0^{th} –order) and a light beam diffracted by the mask pattern (1^{st} –order). While the illumination angle is chosen to balance the pathlength of these two beams, their light intensities are not balanced and exposure latitude (i.e. the insensitivity to dose variations) is reduced. AttPSM with the correct transmission value can be used to rebalance the intensities of the 0^{th} and 1^{st} diffracted orders and are used in this strong-RET to restore exposure latitude.

The illumination angle in OAI is optimized for a given mask feature pitch (Equation 13). Thus feature pitches significantly different than the pitch for which the illumination was optimized will see much less resolution enhancement. To overcome this problem, sub-resolution assist features (SRAF) are added to the layout [6]. These SRAF are dummy features that are drawn into the layout at a dimension where they optically mimic the diffraction angle of the pitch for which the illumination was chosen, but they are below the dimensional resolution of the lithography system so as to not leave an image in the photoresist.

While OAI and attPSM impose no layout restrictions, the need to add SRAF to the layout increasingly requires SRAF-enabling design rules. The layout shown in Figure 8 presented an acceptable SRAF solution for the 130nm technology node [7], however, the hole in the SRAF coverage just right of center in the layout and the general inability to reconstruct an orderly diffraction grating, will cause significant loss of resolution enhancement for more aggressive applications like the 65nm technology node. The most common one-dimension SRAF restriction is the 'forbidden pitch', i.e. pitches that fall in the transition regions between adequate SRAF coverage. Several variations on OAI-attPSM-SRAF have recently been proposed, including double dipole lithography (DDL) [8] and chromeless phase lithography (CPL) [9]. These solutions derive their resolution enhancement from OAI and require the same layout considerations that arise from adding SRAF to a variable-pitch layout.

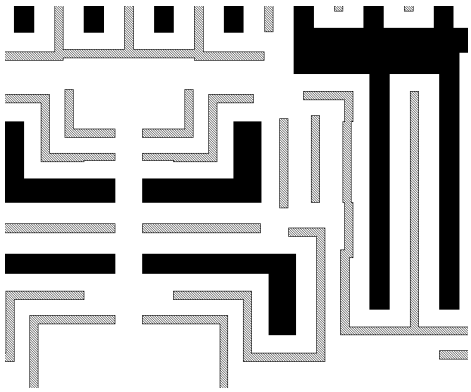

Figure 8 Sraf-enhanced layout showing local sraf conflicts

3.5 Implications

Based on the preceding discussion, the microelectronics industry must adopt strong, highly optimized RET as the lithography solution for all future optical technology nodes. Further, there are no 'miracle RET cures' that avoid layout restrictions. RET-enabling design constraints are the result of tradeoffs between lithographic process window, mask manufacturability, and layout impact. The extremely tight tolerances called for by the 65nm and 45nm nodes leave very little room for lithography tradeoffs.

4. Methodology Impact of Strong-RET

4.1 DRC Shortcomings

Unfortunately, layout constraints required by strong RET cannot be described or enforced through conventional design rules without being unduly conservative [10]. We illustrate this problem here based on altPSM. A design rule to prevent the phase conflict on the simple layout (known as a 'belt buckle') shown in Figure 9, would have to express the equivalent of: "Avoid critical (i.e. needs RET) line-end surrounded by critical lines with lateral spacing < (2*Phase-Width + Phase-Space) on both lateral sides and < (Phase-Width + Phase Space) at end."

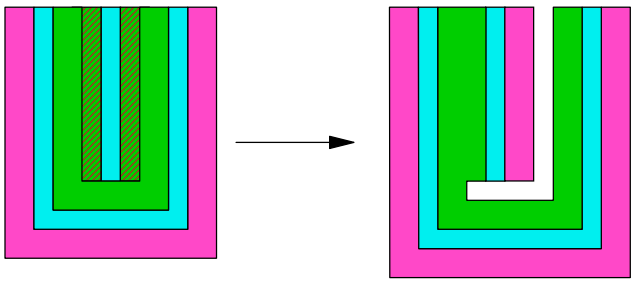

Figure 9 Simple layout forcing complex design rule

This layout restriction is difficult to understand and very phase-parameter specific (and therefore linked to a unique process and altPSM implementation). Simplifications of the layout rules cause inaccuracies that lead to frustration in the layout legalization process. More complicated altPSM errors involve odd-cycles of

phases that span many layout features and cannot be predicted even with the most complicated DRC.

Since conventional methodologies, as illustrated in Figure 3, are enabled through design rule checking, and strong-RET require layout restrictions that can not be captured by conventional design rules, new methodologies are needed for future technology nodes.

4.2 RET-embedded Design Flow

One option, referred to herein as the 'RET-embedded design flow' is to enforce layout compliance with strong-RET by moving the RET design upstream in the flow as illustrated in Figure 10. This flow puts the RET design tool directly in the hands of the designers, thereby avoiding the abstraction of RET layout constraints to conventional design rules. Compliance is verified by achieving a layout without RET conflicts rather than via DRC.

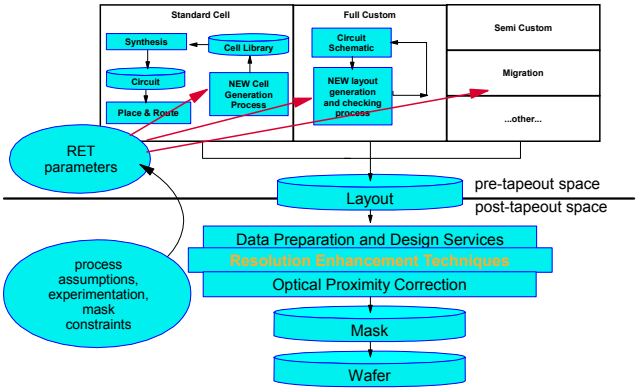

Figure 10. Illustration of RET-embedded layout methodology.

This RET-embedded approach presents several challenges. First, committing to a set of RET-parameters long before mask and wafer processes are established (typically start 2-2.5yrs after design starts), bears the risk of optimizing to a changing specification. Second, the process-specific nature of RET-specific optimization does not ensure layout compatibility with future lithography solutions thus limiting the layout to one technology node. Third, while significant layout effort is required to make designs RET-compliant (feed-back from the RET tools is much more abstract than from conventional DRC tools), general manufacturability [11] is not directly addressed. However, this paper focuses on layout methodology challenges, described next.

4.2.1 Impact on Custom Cell Design

A major challenge facing designers using this methodology is the fact that layout conflicts, such as the phase-error illustrated in Figure 11, do not suggest a correction as conventional design rules do. The RET tool, in this case the altPSM design tool, reports a layout conflict, but it is up to the designer to manipulate the layout to eliminate the conflict. Some work has been done to improve the cause-and-correction relationship in altPSM design (12), but no fully workable hint-function has yet been developed.

4.2.2 Impact on Placement

The long interaction range of most RET solutions (phase interaction distance is about 5X minimum feature spaces, or approximately 5µm for 65nm designs) requires actively preserving RET-compliance during chip assembly. Failure to do so will lead to conflicts as shown in Figure 12. Short of a RET-aware placement tool, RET-compliance can be ensured either by enforcing large exclusion zones around each cell or by enforcing RET boundary conditions. The former has devastating impact on layout density and the latter adds complexity to the already complex problem of layout legalization in the cells.

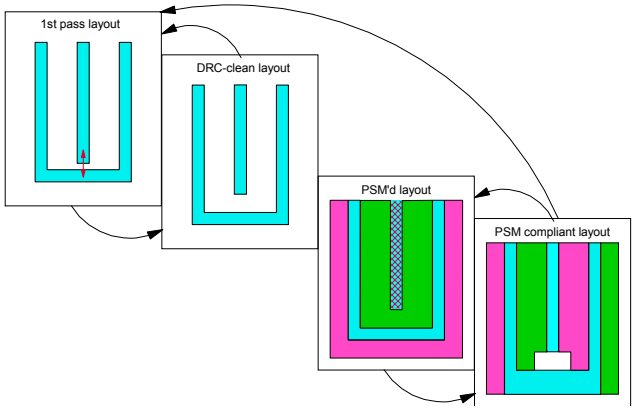

Figure 11. Example of cell level RET-embedded layout flow

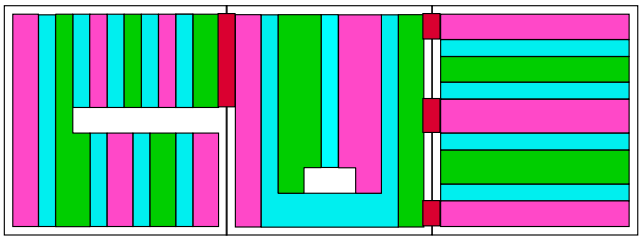

Figure 12. 3 phase-shifted cells with placement-induced conflicts.

4.2.3 Impact on Routing

Typically, the first mask level that needs strong-RET is the poly-conductor level. Since most methodologies prevent cell-to-cell wiring on minimum dimension poly-silicon, RET-aware routing has not been a big issue. However, increasing integration will require strong RET to the metal wiring levels, thereby producing challenges for RET-aware routers as illustrated in Figure 13.

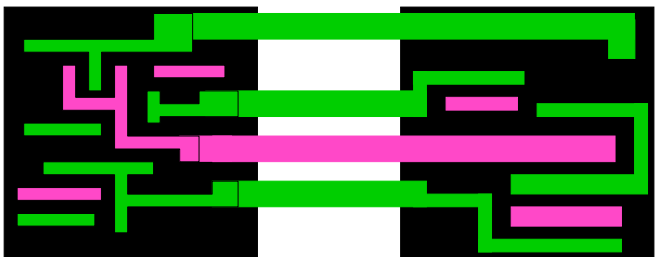

Figure 13, Illustration of challenges for RET-aware routers.

One example of a strong-RET applicable to critical dimension metal levels is dark field altPSM, an altPSM technique for the poly conductor level. In dark field altPSM phases are assigned to drawn shapes which, for commonly used processes using positive resist, end up as mask openings. After resolving phase conflicts in design blocks and enforcing placement boundary conditions, a PSM-aware router has to connect a wire of appropriate phase to phase shifted metal shapes on both ends of the wire and maintain legal phase coloring (two closely spaced wires have to have opposite phase) over the length of the wire. To address this issue, an RET-embedded layout flow can include phase-design capability into the router, thereby adding algorithmic complexity.

4.3 Radically Restricted Rules

4.3.1 The Design for Manufacturability Mantra

The above-mentioned issues can be addressed by requiring layout design-rules, tools, and methodologies to:

- **Generically enable lithographic RET.** A layout that is optimized for many strong-RET avoids problems associated with early commitment to a specific lithography process
- **Improve manufacturability at aggressive patterning resolution.** A layout that does not rely on tight control of 2-D detail will overcome two-beam lithography limitations.
- **Ensure designs can be migrated to future technologies.** The investment in a new layout requires reusing designs for multiple technology generations with minimal redesign effort
- **Allow for density- and performance-competitive chip designs.** Lithography-optimizing constraints that erase the benefits of upgrading technologies node do not make sense
- **Address a broad spectrum of customer objectives with a single design and process.** A common process solution is needed to leverage mask and wafer cost.

These objectives can be met by moving from a 'minimum perturbation' approach to a 'radical design restrictions' (RDR) approach [12]. By clearly communicating fundamental aspects of the patterning process (e.g. resolution is driven by feature pitch) and fundamental goals of the design (contacted device pitch is the main chip density driver in layout front end), compromised rules can be derived that fundamentally improve manufacturability.

4.3.2 Methodology Impact of RDR

A major benefit of 'radical design restrictions' is the dramatic simplification of the layout methodology. By capturing the 'Design for Manufacturability Mantra' in a set of very restrictive yet easily communicated rules, the established, DRC-enabled layout methodology can be preserved as illustrated in Figure 14.

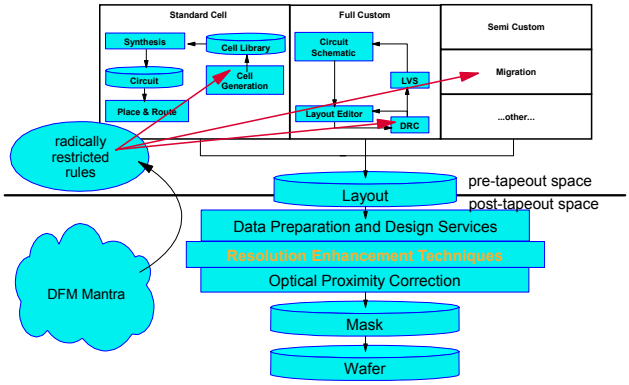

Figure 14. Flow based on 'radically restricted design rules'.

Rather than specifying forbidden pitches and ruling-out complex 2-D constructs, designs are restricted to allow critical dimension features only in one orientation at integer multiples of the contacted device pitch. As the example results in Figure 15 show, a fundamental redesign, involving re-routing the power supplies, can achieve equivalent or better layout density (right) compared to the much less manufacturable, unconstrained layout. The original layout (left) poses many challenges (tight corners, 2-D environments, etc). Addressing these issues by manipulating the CAD polygons causes significant density impact (center). A rigorous redesign achieves all DFM objectives at high density.

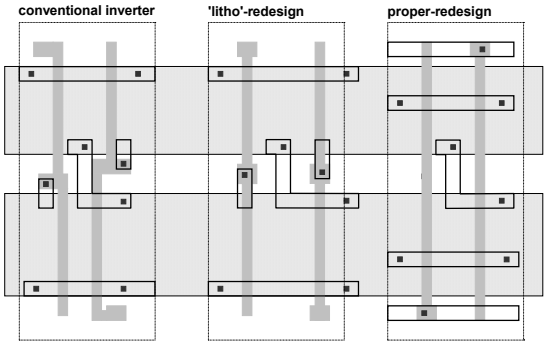

Figure 15. Optimization at design (right) and layout level (center)

Generic RET-compliance is also important for migrateability as is illustrated in Figure 16 on a high-performance, high-density latch design. The radically restricted layout is inherently optimized for all strong-RET, greatly simplifying RET legalization. Note that similar principles apply to dense memory arrays.

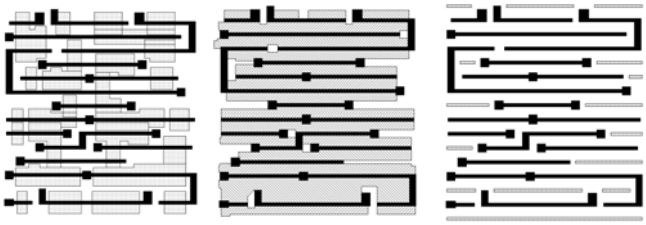

Figure 16. Latch cell designed with RDR (left) is altPSM optimized (center) and OAI-attPSM-SRAF optimized (right).

4.3.3 Placement

As shown in Figure 17, a fully gridded layout methodology greatly reduces the complexity of RET-compliant cell placement. In a layout where all critical features are placed on a coarse grid, the RET solution, in this case the altPSM layout, is independent of device design. As a result, the RET-layout is identical for all cells and placement rules can be easily established without embedding RET knowledge in the placement tool.

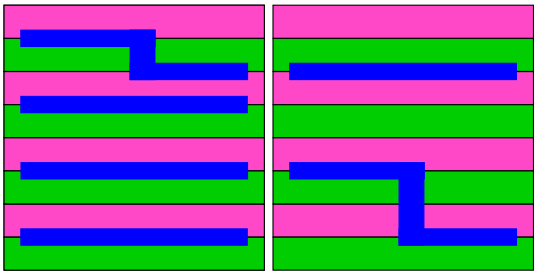

Figure 17. Gridded-layout placement.

4.3.4 Challenges

While the DFM concept is intuitive and provides key benefits to future technology nodes, the following challenges lie ahead:

- **Multi-level optimization tradeoffs**. E.g. avoiding wrong way poly-conductor shapes moves more local interconnect to the first metal level and may increase its complexity; and
- **Multi-parameter layout optimization.** Balancing the needs of RET-enabled lithography, random defect yield, layout density, and chip reliability is not trivial. Even if each need is addressed with first-principle 'rules of thumb', many trade-

offs exist, e.g. lithography needs would indicate diffusion level largely rectangular with no small jogs near critical gates, while electro-migration would dictate multiple redundant contacts with extensions on diffusion shapes.

- **Non-technical challenges.** 'Selling' the DFM mantra to fabless companies that often judge foundries by the aggressiveness of their design rules will be a challenge.

5. Conclusion

Optical lithography is approaching a serious wall. While mild-RET solutions have been sufficient and transparent to designers so far, these solutions are insufficient for 65-nm technologies and beyond, and no adequate lithography tools will exist. Strong RET solutions will thus be necessary, but they require layout restrictions that is cannot be effectively covered by conventional DRC. This paper has described two design methodology options to address this issue: RET-embedded design flows, and flows based on radically-restricted rules. RET-embedded flows are significantly more complicated than conventional flows, and affect cell design, placement and routing. Radically-restricted rules impact designers' actions, but result in lower dependence on strong RET and preserves DRC-based methodologies.

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