Patterning Design Rules in-absolute and on-silicon

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Abstract
PDR based requirements in dimensional metrology are discussed, highlighting the differences between design and patterning and naming the gaps in our ability to support today's RETs, accurate patterning models and PDR validation. It is expected that, once we migrate from CAD based DR definitions (in absolute) to the more realistic PDR definitions for lithography at low K1, uniform dimensional metrology at design, pre-TO and post-TO PDR validation will establish WYSIWYG (what you see is what you get) correspondence between design and silicon.

1 Introduction

The need to decrease critical dimensions (CD) of the most advanced microelectronics devices increasingly challenges our views of the practical limits in optical microlithography. Proliferation of "sub-wavelength" optical lithography has obsoleted WYSIWYG paradigm in layout-to-silicon feature replication. Reticle-based image/pattern enhancement techniques (RET) enabled reduction of the largest systematic intra-field errors. Such changes to "as designed" pattern (on reticles) improved device performance and yield, extending processing margins achievable with optical lithography. Improved size tolerance, in turn, made it possible to print smaller devices. Yet, our industry's slow acceptance of the new design, patterning, and processing methodology is a factor in delaying introduction of the significant potential technology gains. Slow acceptance of aggressive RET is, to be sure, largely a reaction of the design, integration and test/yield communities' apprehension of the risks inherent in rapid proliferation of any new technology.

RETs, especially computer based aggressive modification of design can take such risks to an extreme. Numerous accounts of patterning failures and marginalities are found in the recent literature. Even a cursory review of the recent publications at SPIE Microlithography and Photomask meetings highlights many RET applications that should be classified as something that is between sophisticated frills and demonstrably wasteful changes of the design DB. Panel Discussion at ISQED 2002 clearly suggests the existence of a gap between industry groups that strongly advocate an all-out EDA-lead change of the industry design and manufacturing practices and business models vs. shrewd practitioners of microelectronics manufacturing who take hot-headed proposals to extend the envelope of their POR (process of record) with a grain of salt. They may see the rate of change being too fast, insisting on full-depth risk assessment they used to have. Interestingly, a very recent industry survey of the systematic non-particle functional bin losses [2] reports decrease in the technology-limited yield of CMOS technology as it evolved from CD~500nm to 180nm. This suggests that multiple accounts of isolated cases of failure due to weak links in design may be a part of a much broader trend, implicating a growing deficiency of our design and integration practices, and of design validation.

We may well be violating every DR there is, but we would not know. The reason is simple: we have long run out of capability to validate DRs by 100% inspection and dimensional metrology. Today's best design validation method is said to be yield - too little learning - high price.

This paper reviews basic definitions in dimensional metrology and how we use dimensional metrology (and functional test based data) to design OPC or other RETs. It illustrates generic (typical in our industry) Patterning Design Rules and nets out a minimal set of dimensional metrology capabilities required for today's design and design validation.

PDR based dimensional metrology infrastructure, missing today, coupled with design/function-based metrology and appropriate metrics of PDR compliance, can support the model-based WYSIWYG design, integration and design validation, a solid foundation for "deep sub-wavelength" patterning and efficient microelectronics manufacturing.

2 Digital IC, Lithography and Design Rules

Digital ICs may be the most commonly manufactured microelectronic products of today. Microlithographic patterning of ICs, on the other hand, retained many similarities with analog (objects and their recorded images are of continuous tone, with infinitesimal variations of tone, size and shape) microphotography of 1950s. The built-in expectations of product requirements, materials properties, processing and manufacturing environment are hundreds years old.

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Required to be either fully ON or OFF binary devices are relatively forgiving of manufacturing tolerances. This property enables an efficient mass-production of high yield/performance products that are both reliable and inexpensive. The tightest tolerance required is in matched transistor pairs, preventing the circuit lock-up and/or inappropriate change of state. This requirement is served by symmetry-based (translation, mirror, point) cell replication in IC design, instancing. Efficient IC manufacturing is only possible when every its aspect maintains symmetries required by devices.

If an IC were just a massive array of near-perfect transistors, it would be easier to make. But, to provide complex functions, IC must generate its own pulses to many registers' triggers, amplify and invert signal etc. Transistors that serve such functions are much less numerous, but, because they are designed to match multiples of other devices, their being built to size is also critical. The further away one device is from another, the less matched they may be without any losses. All devices in a die are sized and toleranced according to their design/function. Sizing requirements, reflected in Pattern Design Rules, repeat on the next die – from matched pairs to circuit neighbors, small vs. large etc.

Imaging with optics, unlike pattering with many other means, is a nearly perfect match for the need: imaging properties change slowly as the function of distance, that is to say, locally translation invariant. Unfortunately, local mirror symmetry of optical imaging systems is broken by both asymmetric aberrations and illumination. Point symmetry is broken by most aberrations and anisotropic in-plane image vibration during exposure on scanners. In order to make devices that rely on more than local translation invariance, all optical lithography systems are designed, built and maintained as free of errors as possible. Optical microlithography enables manufacture of devices that are near- perfectly matched over small distances and very well matched over the whole field. Any device features on the reticle, either isolated or in uniform array (period down to λ/2NA), are replicated with near-perfect uniformity (small variance).

Simultaneously correct sizing of both small and large features, on the other hand, is somewhat difficult due to optical diffraction and interference effects. Significant variation occurs for features in varying proximity of each other and at the end of a uniform array >λ/NA distance is required (wasted) to either prevent or compensate such changes in imaging. To sum up: optical lithography may be the perfect match for the manufacture of uniformly sized and spaced devices. At its incoherent cut-off limit, it allows printing close to one device per (λ/2NA)*2 area on the wafer. Optical microlithography at 248nm (in air/no frequency doubling) can pattern devices at half-pitch of 64nm, with device CD being much smaller.

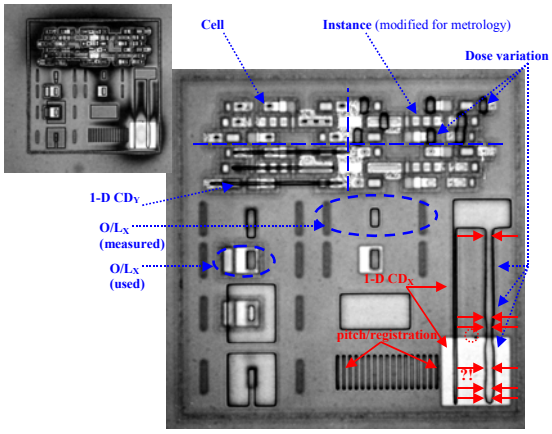


Figure 1. Metrology Test Site [1] in bright field with (insert) NA=0.2, λ=546+/-5nm and NA=0.9, white light.

Printing on the previously patterned substrates, illustrated in Fig. 1, may further degrade the device replication by optical lithography or it may retain it, if at a price. It may also be forgiving of error (self-compensating), reducing sizing errors accrued in the device patterns. The outcome is a strong function of layouts and patterning processes.

Prevailing design and manufacturing practices of today severely limit the ultimately achievable device tolerances by requiring that all features – any shape, size, polarity, orientation, regardless of proximity – be printed "to size". Although much better patterning and device performance can be achieved through design and process integration, limitations of this kind are not obvious at design, let alone what it will cost to manufacture "as designed" or what gains we lost by failing to explore alternatives.

To better account for actual device needs, to reduce the waste inherent in the indiscriminate requirement for tight sizing and the loss from not allowing something critical to be as tight as can be and loosing yield or performance, we use ***Patterning Design Rules***. These Rules must be based on the designers' knowledge of the design/device function. They must also account for patterning processes and our ability to control them and to assure compliance. It is of essence to understand **PDRs**, with all aspects of IC manufacturing embodied in them, from basic physics to trade-offs in performance and yield, manufacturability, costs etc. Improving device tolerances as required by PDRs, as well as improving PDRs themselves, is required for a new design and patterning methodology to emerge.

3 Design Rules and Dimensional Metrology

Design Rules is a normative document that specifies the key dimensions of a product that may be manufactured, while staying within known capabilities of a generation of lithography and patterning equipment, supported by everything required to produce an IC – from design and design validation methods and tools, to materials and processing, metrology and process control, failure analysis etc. In a sense, a set of Design Rules embodies our collective wisdom. They may look less than glamorous, but when followed, gross deficiency of a new product is unlikely. A product may be designed, design validated and chips manufactured - with product properties being predictably close to the expectations. As in any well-run business process, each Design Rule is reviewed in the light of the recent learning. A new or a tighter Design Rule may be needed to preclude marginal design that lead to yield loss. A Design Rule may be removed/relaxed when it is established – with certainty - that losses of anything tangible do not occur when it is violated, especially when relaxing this Rule leads to quantifiable tangible gains or to recognizable non-tangible gains.

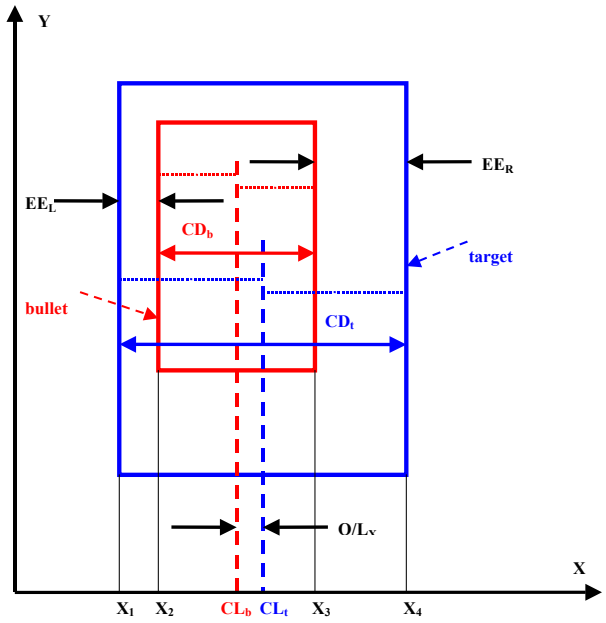


Figure 2. Linewidth (CD), centerline (CL), overlay (O/L) and edge-to-edge overlay (EE O/L).

To define Patterning Design Rules, and its counterparts in dimensional metrology, we use broadly applicable convention [1, 3-5] illustrated in Figure 2. We use the name feature to denote the simplest element in one layer of the design of a thin film device. Feature linewidth (space width, width, critical dimension or CD) in layer t (target, reference) and level b (bullet, resist, current) is denoted CD_t and CD_b, respectively. If the edge coordinates are denoted as X_1, X_2, X_3 and X_4, then

$$\mathbf{CD_t = |X_2 - X_3|}$$

and

$$\mathbf{CD_b = |X_1 - X_4|.}$$

Likewise, the centerlines of the target and bullet featuresare denoted CL_t and CL_b,

$$\mathbf{CL_t = (X_2 + X_3)/2}$$

and

$$\mathbf{L_b = (X_1 + X_4)/2.}$$

Since microlithography involves patterning very many features in each layer, a set of all centerline coordinates, registration, is of interest when it pertains to in-plane distance between a centerline of a feature in one layer and a feature in another layer, used as reference. This distance is centerline overlay (overlay, O/L). Referring to Figure 1, overlay of two features, whose centerlines are CL_b and CL_t, is defined using the following convention:

$$\mathbf{O/L = CL_b - CL_t.}$$

PDRs require that certain widths in certain features be within stated allowed ranges, manufactured to size within stated tolerances. Accurate account for EE O/L is required for effective design and integration of IC patterning. Failures to comply with EE O/L PDRs in back end of the line (BEOL, metallization) are known to lead to poor yield and reliability. Metrology of device O/L and EE O/L, see Fig. 1, was developed [6]. It is on the SIA and SEMATECH Roadmaps since 1994. Yet, in today's practice, device level O/L, especially EE O/L, is seldom measured [7]. Designers' assumption that dimensional metrology is readily available and used to validate PDRs, as used at design and pre-TO validation, is violated.

Today's design environment still has, or appears to have, a complete account of all dimensions of all features in all layers. Design and integration universally recognize that "over-design" leads to lower profits, that "under-design" is a risk that may result in loss of product yield and/or reliability. We know that the best-designed product does not fail at "a single weak link" – it does not have one. When stressed to fail, the best-designed product will fail everywhere at once, reaching the highest stress limit. To achieve that, our design practices shrewdly prescribe where the tightest DRs may be used. Designs are thoroughly evaluated to make sure that if the tightest DR is used in just a few layouts of a product, these be re-designed and relaxed or the rest of the product also take full advantage that stems from using that tightest DR. Yet, our design and design validation environment is largely oblivious of the diverse environments in imaging, image recording and image transfer for one layer on a virgin substrate, let alone on a previously patterned and processed wafer. Assumption that the design is uniformly replicated on the wafer and that the product is compliant with the design, within tolerance, is no longer true.

Low k_1 optical microlithography brought in strong new interactions of imaging and patterning processes with design. This patterning environment is deluged with unintended variations of both CD and image placement: image placement of dissimilar features is not the same, asymmetric aberrations and illuminator errors move image laterally through focus, errors of OPC or assist features, of phase, transmission, size or placement of phase shifters result in variations of both CD and image placement. What may be the least recognized is that potential improvements of pattern tolerances and process windows, the goal of RET, are only possible to the extent that their integration may reduce the total of all patterning errors. The success or failure of microlithography is not dependent on improved image "resolution" or "fidelity". That is predicated by sustained reduction of CD and EE O/L tolerances in device patterning, as required by PDR, on the condition that it is the most cost-effective means to improve product yield and performance.

It is of essence to all of us in microelectronics industry to review and define a set of **generic Patterning Design Rules**, to make certain that standard PDRs are supported by **complete and uniform dimensional metrology** tools in every key aspect of model-based WYSIWYG for design and integration:

- accurate patterning and processing models;
- function-aware metrology for design and pre-TO PDR compliance validation;
- function-aware metrology for post-TO and in-production PDR compliance validation;

Referring to critical layers in CMOS and bipolar ICs, here is a short list of generic PDRs [1]:

One-layer Design Rules

- 1-D line/space **width** (same for 2-D), with **widest/narrowest** width between opposing edges in one layer;
- 2-D island/trench also require **area, perimeter, aspect ratio** and, possibly, radius of corner rounding.

Two-layer Design Rules

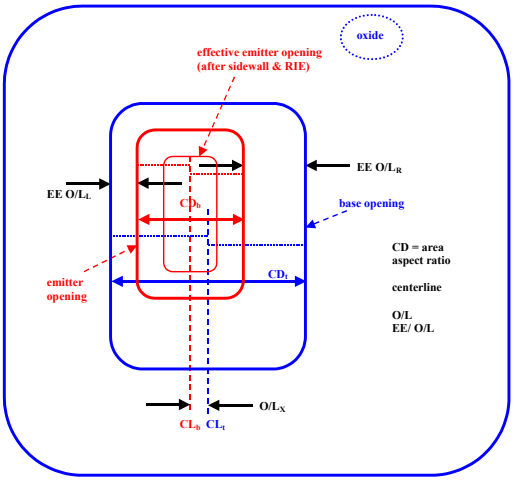
- 1-D line/space widths (same for 2-D) etc., but only for the portion where one pattern is over another;
- feature-to-feature-in-another-layer overlap (area that is common to both layers);
- **EE O/L**, 1-D measure of overlap between two edges (same sense or opposite) of different layers.

4 PDR case study: 2-D feature (emitter or contact)

This is an illustration, and discussion, about what is and is not important in patterning ICs. It highlights the key aspects of model-assisted design environment in the case of the simplest serif-based OPC [8]. This OPC is commonly used at contact, via and implant layers, as well as emitter of bipolar devices. This old example has no proprietary aspects and is exceedingly simple, making it easy to observe and discuss the issues.

Problem statement:

Rectangular and substantially isolated emitter openings fail to print to size across all emitter sizes allowed by the Groundrules. When exposure is such that large rectangles are "on target", rectangles with smaller side <λ/NA are undersized; percentage area loss is the worst for squares. Since the sidewall narrowing technology is used to shrink emitter area, this poor size tolerance is applied to a much smaller effective emitter area. Bipolar transistor design and PDRs of relevance are illustrated in Figure 3; a great deal of salient detail related to these generic DRs is



available in the public domain [9]:

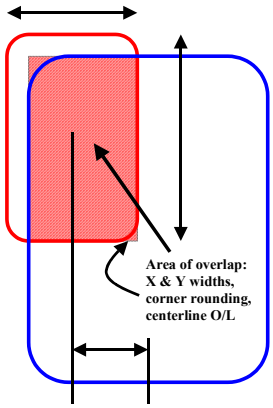


Figure 3. PDRs for emitter opening in bipolar transistors. Design is Fig. 2. Printed resist pattern is shown in Fig. 1.

Design #1: non-aggressive serif

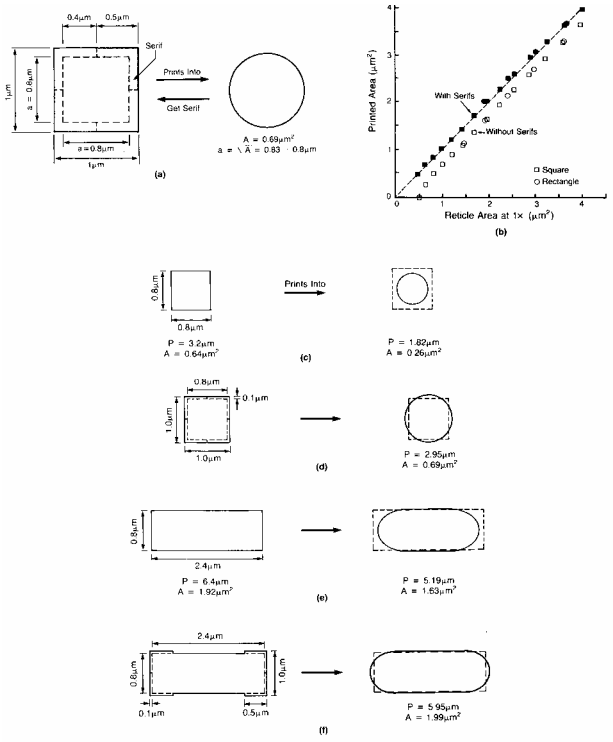


Figure 4. Design and properties of non-aggressive serif.

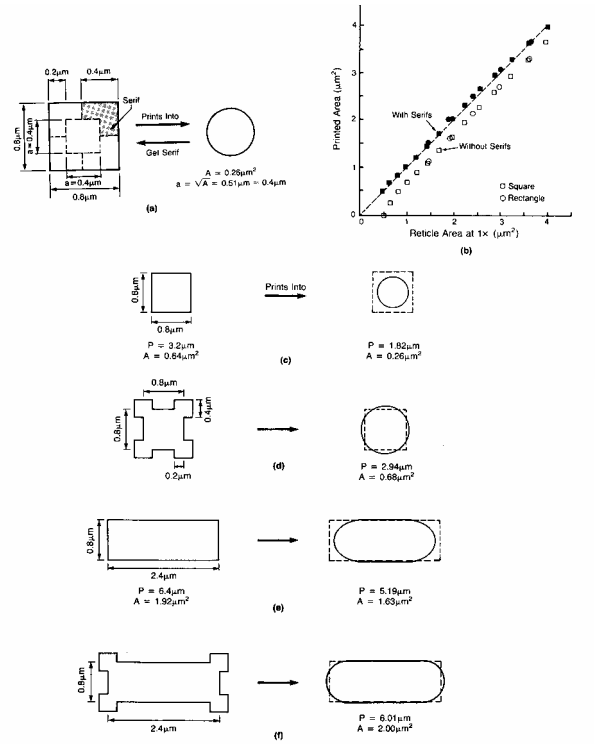


Figure 5. Design and properties of aggressive serif.

Although designers **want** emitter printed as a rectangle with aspect ratio ~1.5 (so densely packed transistors may drive as high a current as allowed by the current density), they **need** all designed emitters printed close to designed size, with tight control of **area** for each type.

Quest for best RET (introduction to dialog):
What is "optimal design"? What is "designer intent"? What are design objectives? How should the many conflicting requirements be co-optimized?

A square is the **least complex shape** on the design grid. A model of lithographic printing shows that a single size square serif gives some improvement of areas printed for rectangles across a broad range of sizes and aspect ratios, as needed. This is a two-parameter design (serif size and extension/jog). It involves one or two experimental data points and a "back of the envelope" design procedure and model-based assessment of variable of area, perimeter and aspect ratio correction at "aggressiveness"; Figs. 4-5.

Design must be validated - the means may not exist. Which design is easier to manufacture on the reticle? **Model-based evaluation** of impact, such as influence of mask sizing error on sizing in print and on defect printability: the more aggressive serifs, the stronger impact.

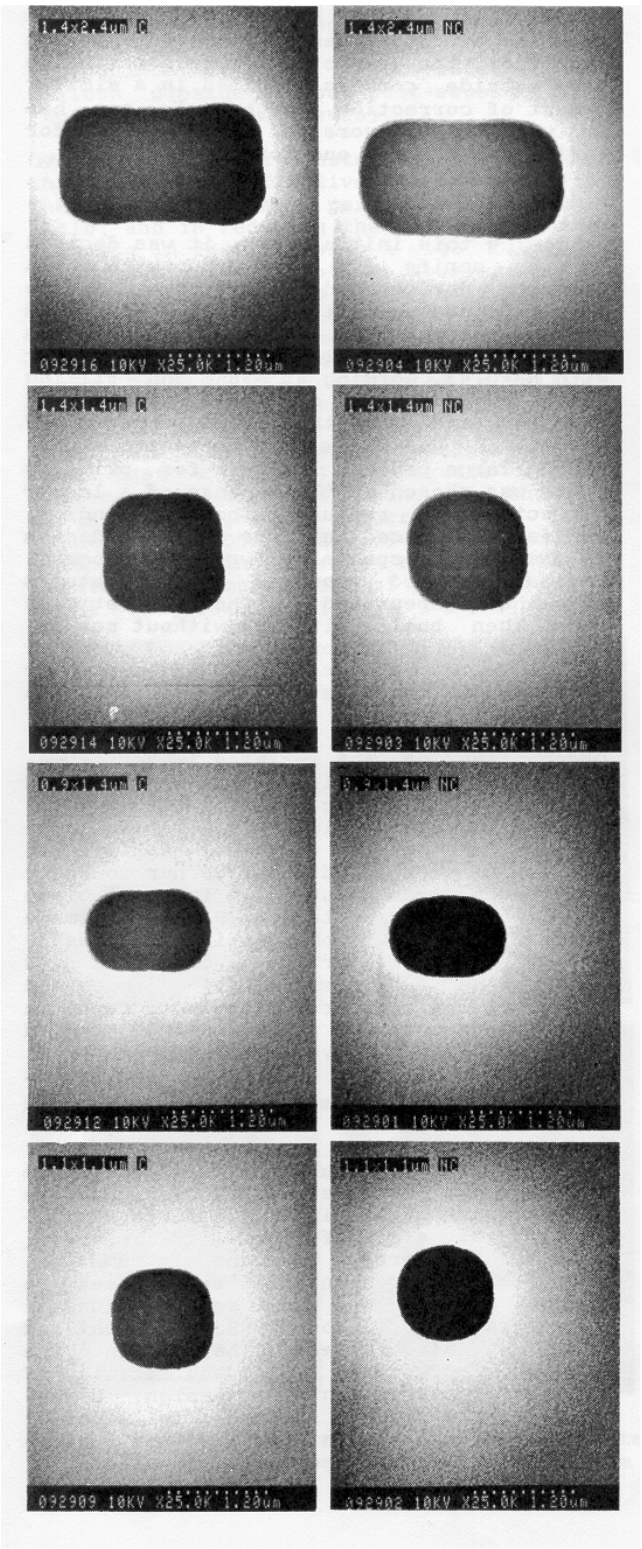
Design #2: aggressive serif

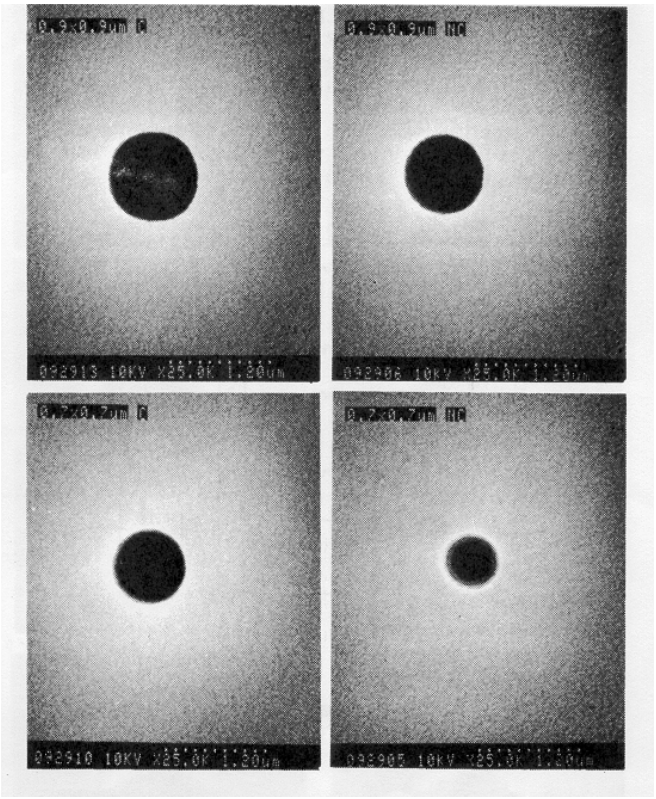
Which design gives closer size to target?
Which design leads to smaller variance at each size?
Both aggressive and non-aggressive design result in print area, perimeter and aspect ratio brought up to near target for all features. **But…** aggressive design has poor process windows, driving high variance (Fig. 8).

Which is a better design?
What are the metrics?
Is the model accurate?
How accurate is metrology?

Need metrology of area, perimeter and aspect ratio.
This is the DR at stake here – better control of this parameter, **area**, indicates success. Build and print reticles (POR). Measure area in print, Figs. 7, 9-10. Use estimated error to improve the design. Correct inaccuracy during model use in RETs (and model-based pre-tape-out validation). Dimensional metrology (of area in print) and electrical test data (cross-checked and self-consistent) - not the model - are the inputs to model-based design procedure (rule, algorithm).

Pre-T/O design validation requires accurate models.





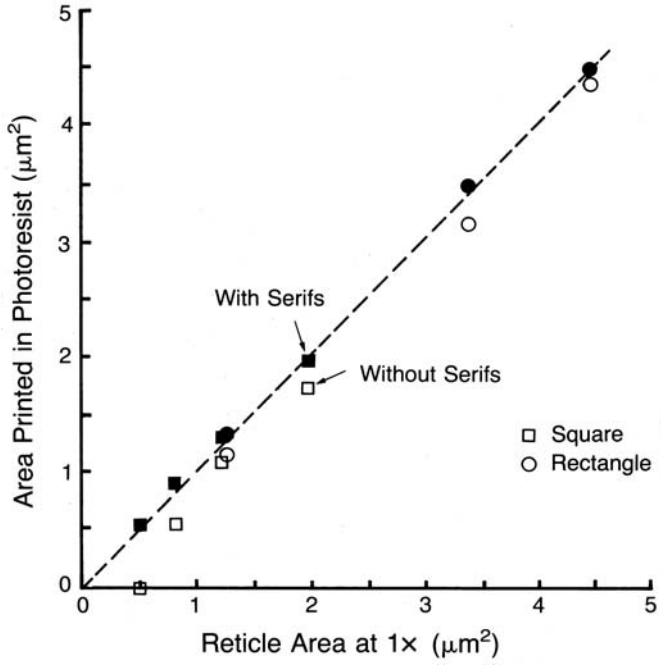


Figure 7. SEM based metrology of area in print.

Post-tape-out design validation requires metrology. Metrology of area (with a specially modified SEM) shown in Fig. 7 confirms that emitter openings with serifs print closer to target sizes across a wide range of sizes and aspect ratios. This is manual, laborious and not all PDRs are checked – no capability. This alone is not enough – must confirm over process window.

Dimensional metrology of emitter size in Fig. 7 and, more to the point, **e-test of effective area** in Figs. 9-10 confirm that emitter openings with serifs print closer to target and (even) with improved distributions.

This is just begins to validate the utility and PDR compliance for *isolated small 2-D features*…

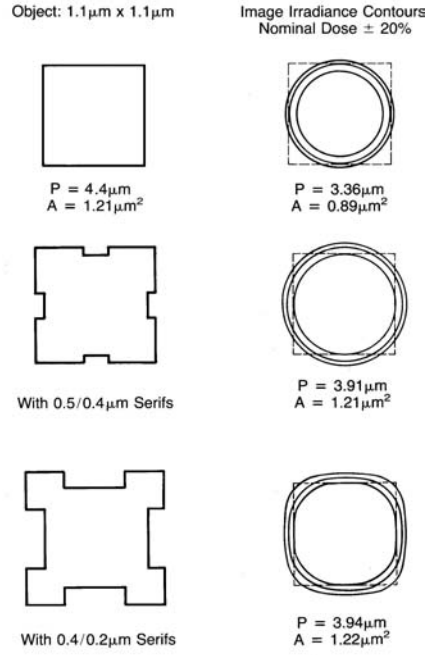


Figure 8. Engineering trade-offs in aggressive serifs.

5 Summary and Recommendation

Dimensional metrology capabilities of area and perimeter in small 2-D features do not exist even today. 1-D CD and aspect ratio can be measured [10].

Standard definitions of PDRs do not exist and, as the result, dimensional metrology capabilities to support them as required in low K1 patterning do not exist, either.

Some functional test based assessments of patterning are available [11]. The best PDR validation we have is yield.

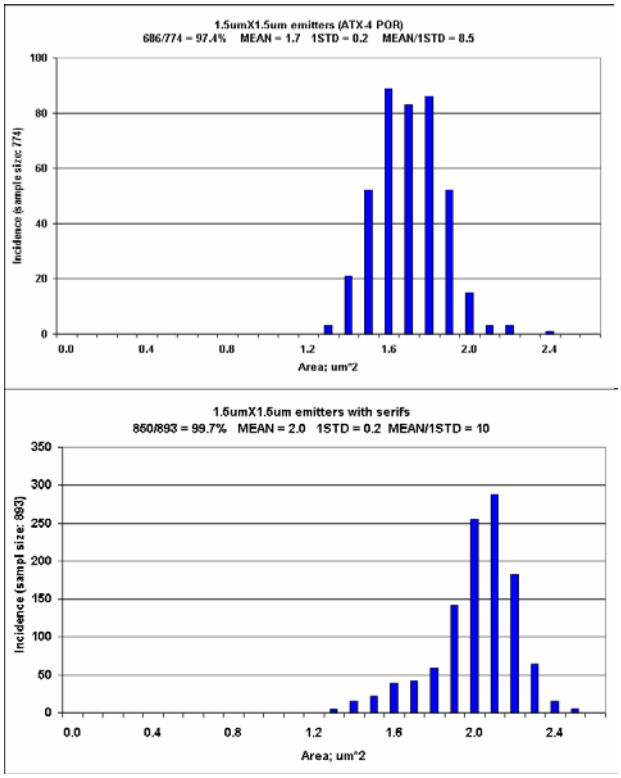


Figure 9. Large emitters with serifs are closer to target and tighter distribution (mean/STD).

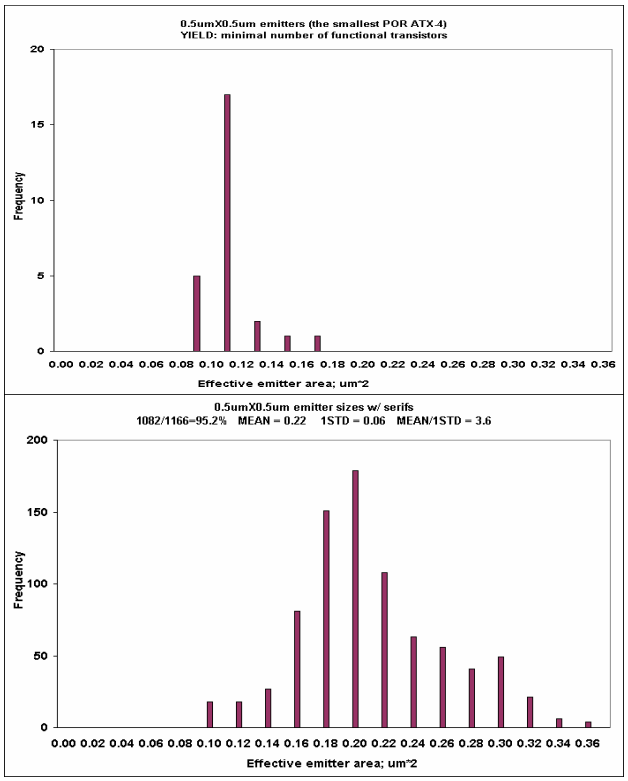


Figure 10. Small emitters without serifs are grossly below size and failing.

PDR based dimensional metrology in model images and on wafers is required for sustained improvement of competitiveness and health of our industry.

Required dimensional metrology can be developed.

Effective dialog between designers, lithographers and metrologists is needed to arrive at consensual definitions of Patterning Design Rules. This is the message of this paper to the design community. It is also an invitation for our colleagues, industry-wide, to co-define PDRs, to discuss them in the leading technology forums and to publish them in the open domain.

This author, with several colleagues already joining, plans to take this subject to ***In-Depth Seminar*** at SPIE Microlithography 2004. The output will be published as a consensual ***Program Paper*** such as [12].

Our involvement with the suppliers, co-developing the new standard PDR-related dimensional metrology, may then take place at our industry's microlithography and metrology meetings. This will help the extensions of CD-SEM and CD-AFM metrology to emerge, fuel the development of the calibrated patterning/processing models to account for 2-D and 3-D patterning in microlithography and the emergence of the process-aware model-based metrology-assisted WYSIWYG paradigm for design and integration.

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