# Manufacturability Metrics and RET Tradeoffs For Physical Design and Layout

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**Abstract**

*In the development of technology nodes at 65 nm and below, manufacturability verification must be performed simultaneously with physical design, in order to guarantee sufficient process margins and economic viability. Three fundamental fabrication metrics are presented in this work, together with direct applications on physical design. Algorithms are predicated onto EDA software tools, which allow for the integration of design verification and process simulation capabilities. These novel methodologies enable the first practical implementation of a Design For Manufacturability flow.*

## 1 Introduction

State-of-the-art design methodologies for VLSI electronic systems, in the last decade, have relied upon well-defined, fundamental levels of abstractions, from behavioral and functional specifications to system architecture definitions, from electronic block partitions to device design and, finally, from physical layouts to integrated semiconductor fabrication. Definitions of these design-level boundaries have been enabled and maintained by the continuous scaling rate in integrated circuit manufacturing, commonly referred to as "Moore's Law".

In the deep sub-100 nm domain (65, 45, 32 and 22 nm technology nodes), the entire design hierarchy is being challenged by non-linear effects due both to fabrication processes, and to nanoscale physical phenomena. As a direct consequence, exponential increase in semiconductor manufacturing costs for *traditionally* designed systems, severely threatens the economic feasibility of the entire electronic industry.

Interdisciplinary activities at various levels of design abstraction are converging into a proper R&D area, generally denoted as Design For Manufacturability. This paper will present the core set of these novel methodologies, and their application to the extraction of manufacturability metrics for Physical Design Layouts.

## 2 Design For Manufacturability

The broad field of Design For Manufacturability (DFM) addresses the fundamental VLSI engineering problem, defined in the previous section, by informing electronic design methodologies and tools with rigorous manufacturability knowledge and constraints. Its scope is not limited to the layout design and physical verification levels of the flow, but extends into the architectural and behavioral specification domains [1]. DFM consists of re-mapping the problem of **how to fabricate** a given electronic system into the problem of **how to specify and design** a *manufacturable* system.

Historically, during the development of the 180, 130 and 90 nm technology nodes, the natural (and more obvious) insertion points for DFM methodologies and techniques have been confined to the Physical Verification steps of the flow (*primary insertion point* as depicted in Figure 1). Resolution Enhancement Techniques and Optical (or, more appropriately, Process) Proximity Correction (RET/OPC) have become standard industrial practices in the development of advanced integrated devices. RET/OPC algorithms and software tools introduce local corrections to a given physical design so that economically viable fabrication processes can be employed to meet system specifications. These design modifications often conflict with original design specifications, and therefore RET/OPC applicability is severely limited, in the current traditional setting.

As a characteristic example, adoption of Alternating Phase Shift Mask (A-PSM) technology enables sub-resolution patterning, without expensive reduction in wavelength of the lithographic tools [2]. On the other hand, the use of A-PSM requires a layout to conform to specific geometric constrains. Satisfying such constrains often causes a global geometrical chain reaction, affecting the design all the way from cell synthesis to full-chip place-and-route. Electrical characteristics of individual devices (transistor's leakage currents and threshold voltages) are also directly affected. A vast class of electronic designs is currently not amenable to A-PSM, because implementation conflicts cannot be

eliminated without major (or complete) costly re-design. Furthermore no design automation methodology, nor tool, exists to evaluate the impact of changes in electrical behavior of the system (for instance critical paths, clock skew, etc.), which can propagate upstream in the chain of design abstractions, up to the architectural level.
This example highlights that *a posteriori* verification of manufacturability conditions is not an effective methodology for mapping electronic designs onto current and future fabrication processes. The appropriate engineering solution must consist of the definition of process-aware (or process-specific) design flows and the adoption of fundamentally new EDA methodologies, to be deployed during, and not after, physical design development.

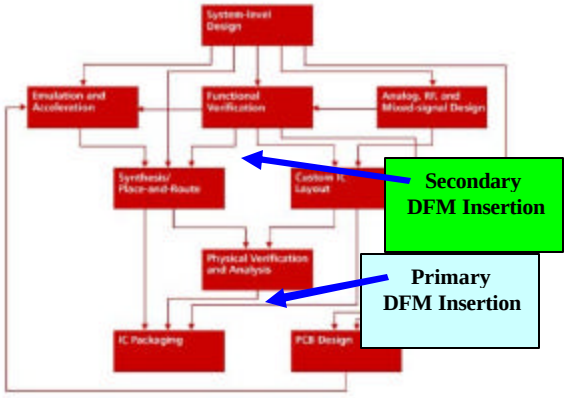


Figure 1: Flow Insertion Points for DFM.

In order to enable a more efficient *secondary insertion point* for DFM (as shown in Figure 1) quantitative manufacturability metrics must be available and integrated into automated layout synthesis and/or manual custom layout. Technical aspects of the implementation of such metrics will be presented in the following sections.

## 3 Functional Model for a DFM Engine

Existing RET/OPC tools provide integrated CAD layout and process simulation functionalities, which can be programmed to build virtually any DFM application. Within the scope of this study, we will describe the most general framework for Physical Design Layout applications, targeting 3 main objectives:

a. augmenting and guaranteeing layout manufacturability with respect to process latitude;
b. analyzing impact of CD variation and pattern fidelity on functional and electrical performance;
c. supporting the selection of a manufacturable Design Rule set.

Objective (c) is particularly critical in the sub-wavelength manufacturing domain. While *classical* Design Rules (DR's) for technology nodes above 130 nm were able to encapsulate most of process behavior and limitations, for 100 nm and below, non-linear effects cannot be described in crude terms of purely geometrical rules. Adoption of Model Based OPC (to replace simplistic Rule Based OPC) is the strongest indicator of the inability of DR's to accurately describe manufacturing processes. If a given fabrication process, in a specific technology, could be completely described with a set of DR's then, for each rule, an appropriate proximity correction action could also be defined. Instead, Model Based OPC (i.e. simulation based corrective actions) must be implemented to fix large classes of layout problems, not captured (nor predicted) by rules.
A further limitation of DR's is that they lack the ability to describe the entire chain of cause-and-effect from imaging to patterning distortions onto single device electrical characteristics and finally onto full chip functionalities. DFM applications are not aimed towards replacing DR's, but rather towards extending them, by integrating non-linear effects at various length scales.

The fundamental building block for a DFM engine is represented in Figure 2.

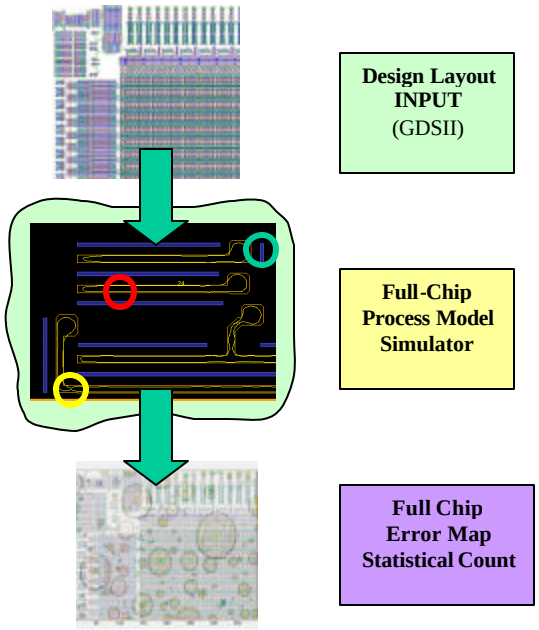


Figure 2: DFM Functional Building Block

It consists of an Image and Process Model Simulator integrated within a physical verification (DRC/LVS) software environment, built on top of a hierarchical design database. A suitable programming (or scripting) language (such as Perl, Tcl, etc.) allows for the development and implementation of specific DFM applications. Computational capabilities of the engine must include hierarchical (and flat) processing of polygonal data, fast process modeling and statistical analysis, including error counting and area (X,Y) mapping.
The ability to extract process **error statistics** at the full chip level, including exact locations for such errors is the true leverage of the DFM engine.
Extraction and categorization of process errors can be based either on edge placement (CD) or patterning and image properties (contrast, image log-slope). Both types of errors can be also evaluated with respect to process latitude, as it will be shown in the following section.

Two general classes of DFM applications can be built using this functional model.
A DFM *Design Analysis Application* iterates over an input set of design layout variants, given a specified process model, and computes a ranking of these design variants based on their respective distribution of process errors.
Analogously a DFM *Process Analysis Application* iterates over a set of process models, given a specified test design layout, and computes a ranking of the input process models again based on the different error distributions generated by simulating each process onto the given test design.

## 4 Manufacturability Metrics

The availability of the functional DFM core, as defined previously, allows for the implementation of novel applications to be inserted during the layout design phase of the flow. This section will describe 3 fundamental manufacturability metrics and corresponding algorithmic implementations. As state of the art in DFM continues to evolve, similar applications will become standard part of design flows.

### 4.1 Design Rule Look-Ahead

The early phases of a technology node development (e.g. 90 nm, 65 nm, etc.) consist mainly of the definition of a suitable set of Design Rules. The starting point for this set is typically a "shrink" version of a previous rule set generation. Since no physical fabrication process has actually been implemented at this stage of development, validation of the manufacturability for each individual rule can only be based on extrapolations of previous empirical data and/or simulated predictions of future processes.
Except for individual (company specific) best practices, no formal methodology is applied at this stage to generate a **quantitative** assessment of the manufacturability of each proposed design rule. As soon as the initial DR's set is released and physical designs are started, a particularly "fabrication critical" rule might therefore be extensively used and become embedded into cell libraries and macros. The discovery of such criticality will occur much later in the flow, for instance during a test chip revision, with severe economic and technological penalties.
The following *Design-Rule-Look-ahead* (DRL) algorithm provides a formal methodology for DR's evaluation. The procedure is based on the fundamental observation that design rules do not exist in abstract, but they are rather "abstractions" (or generalizations) of actual geometrical conditions occurring in real layouts.

DRL Algorithm I [Ranking and Revision]

Given a set of test layouts ($TL_j$) and a set of design rules ($DR_k$):

(1) Perform Design Rule Checks on $TL_j$
(2) Compute $DR_k$ histogram (frequency count)
(3) For each $DR_k$
    a. Perform process simulation
    b. Extract process metrics (CD errors)
    c. Compute Manufacturability Ranking
(4) Sort DR's according to ranking

Typical results of the first two steps of the algorithm are shown in Figure 3. In this specific case 7 designs have been used to extract rule checks and their respective frequency counts (represented as histograms) out of a (synthetic) set of 10 rules.

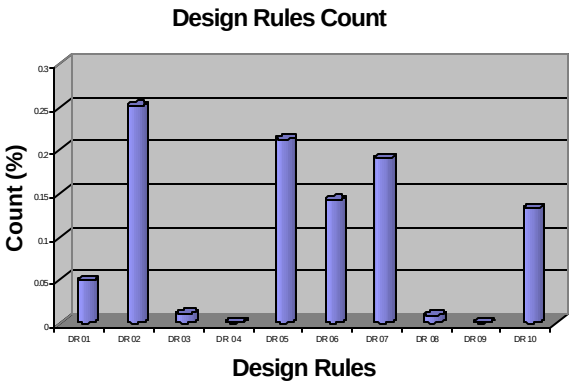


Figure 3: DR's frequencies

It can be immediately observed that $DR_4$ and $DR_9$ have a very low frequency compared to most of the other rules in the set.
As design rule occurrences are checked against the test layouts, corresponding $DR_k$ locations are also identified. This allows process simulation to be performed at each of these locations. It is very important to notice that, in this methodology, a given design rule can be simulated several times, within the different geometrical contexts it appears in. This allows for an increased level of confidence in the modeled fabrication robustness, as a statistical model is implicit in the algorithm.
The Manufacturability Ranking (MR) value in step 3.c can be computed as a function of process errors returned by the simulation and analysis steps (3a, 3.b). Average CD error, for instance, can be typically used.
The final DR's sorting order is obtained by multiplying each $DR_k$ frequency with its corresponding MR. This sorting constitutes also a quantitative *revision order*, which can be used to determine the cost of changing or eliminating a given design rule with poor manufacturability.
In the case depicted in Figure 3, $DR_4$ results to be the first candidate for rule revision, because its large average CD error (fabrication critical) and its extreme low occurrence in the input test layouts (design non-critical).

While the DRL I algorithm allows to quantitatively compare sets of design rules among themselves, thus determining what rule (or rules) degrade manufacturability, the procedure does not provide any indication about what "improvements" could be introduced into a design rule set in order to make it more manufacturable. An algorithmic variant to address this issue will be presented in the following section.

### 4.2 Design-Rule Analysis (Forbidden Pitches)

Any manufacturability metric is obviously not simply a function of a specific DR's set, but also of the chosen fabrication process [3]. This intrinsic dependency stands at the root of a potentially catastrophic flaw affecting all the *traditional* design-to-manufacturing flows, currently adopted in the electronic industry. Design rules tend to be defined at the very beginning of technology node development, when only vague approximations exist relative to the actual production processes of choice. The 65 nm technology node is emblematic. First lithography tools will be shipped by the end of 2003, almost two quarters later than the definition of the actual design rules. But while it is an accepted industrial practice to revise OPC treatments every time a change in the fabrication process is introduced, DR's are very seldom modified.

In order to support DR's revision based on process changes, a variant of the DRL algorithm is proposed. The procedure allows for the characterization of a **Manufacturability Matrix** MM(k,j), where each row corresponds to a given rule $DR_k$ in a DR's set and each column correspond to a fabrication process alternative RETj. MM(k,j) values can be any of the previously defined process error metrics, such as average CD error, image contrast, process latitude, etc.
The algorithm will be applied to the analysis of fabrication sensitivity for a DR's set, with respect to the well-known phenomenon of "Forbidden Pitches" [4].
As shown in Figure 4, Critical Dimension (for gate features in this specific case) displays a strong variability, with respect to its nominal value, functionally dependent on feature pitch.

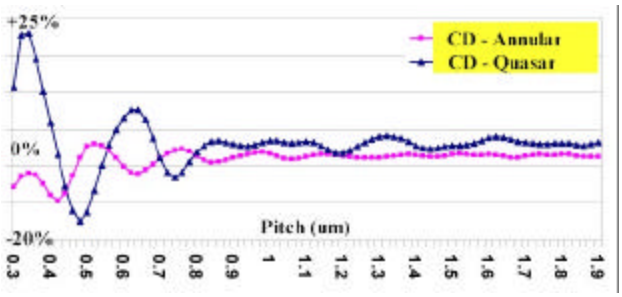


Figure 4: Forbidden Pitches for Annular and Quasar

Furthermore such dependency also varies with different patterning processes as it can be observed for Annular Illumination and Quasar Illumination, in Figure 4. This well known lithographic effect results in some CD's not to be correctable with any type of OPC, because of the extreme oscillation in their magnitude. Analogous pitch effects exist for line ends, corner rounding and in general any type of pattern fidelity measure. It can be concluded that in the sub-resolution domain these types of non-linearity cause manufacturability of layouts and design rules to be completely tied to a chosen fabrication process [5].
The first two steps of the DRL II algorithm are the same as in the original DRL I. Design rule checks are performed on test layouts in order to extract a frequency count for each rule, thus quantifying its relevance for the given technology.
A Manufacturability Matrix is then computed by modifying the inner loop and further iterating over a given set of RET processes. Manufacturability of every layout is carried out first allowing unrestricted pitches in test layouts, then selectively removing the RET specific pitches.

Values MM(k,j) are finally computed as the ratio of a given process error metric with forbidden pitches removed, divided by the same metric simulated with test layouts *including* all pitches.

DRL Algorithm II [Forbidden Pitches Analysis]

Given a set of test layouts ($TL_j$) and a set of design rules ($DR_k$):

(1) Perform Design Rule Checks on $TL_j$
(2) Compute $DR_k$ histogram (frequency count)
(3)
(4) For each $RET_j$
    a. Evaluate set of forbidden pitches ($FP_j$)

(5) For each $DR_k$, for each $RET_j$
    a. Perform process simulation (all pitches)
    b. Extract process metrics ($CDE_1$)
    c. Perform process simulation (forbidden pitches $FP_j$ removed)
    d. Extract process metric ($CDE_2$)
    e. Compute Manufacturability Ranking as ratio $CDE_2/CDE_1$

(6) Sort DR's according to ranking in MM(k,j)

Design rule negotiations among product design groups, process integration groups and fabrication groups can directly apply this methodology for the quantification of the trade-off between the introduction of DR's restrictions and their immediate benefit in terms of manufacturability. For instance, considering process data given in Figure 4, the choice of Annular illumination ($RET_1$) which allows for more general design rules (no forbidden pitches) might be quantitatively compared and replaced by the choice of Quasar illumination ($RET_2$), which requires more stringent design rules (2 intervals of forbidden pitches), but has an overall superior manufacturability ranking (reduced process CD error).

### 4.3 Layout Process Signature

As a further generalization of the methodologies presented in the previous section it is possible to define a *Layout Process Signature* (LPS) metric, as a full chip X,Y distribution of process errors.
Any software implementation of the DFM engine described in Section 3 (Figure 2) can extract not only a statistical count for any given process metric, but also its magnitude at any given point over the full layout.
Figure 5.1 shows an example of LPS. A statistical count of line-end pullback errors has been extracted for a given lithographic process at two values of focus (best focus and best focus -5%). CD error values are indicated on the X-axis, from 0 nm (right of the graph) to negative 60 nm line-end pullback (left of the graph). The Y-axis reports the total count of line-end errors in a given range. It can be observed that when the process is simulated out of focus, the distribution of line-end errors shifts towards an overall reduction in layout manufacturability.
An analogous histogram of line-end pullback errors is shown in Figure 5.2. In this case magnitudes of the process metric are plotted in the 2-dimensional space of lithographic focus and exposure dose. Finally Figure 5.3 correlates the statistical count with the X,Y map over the full layout.

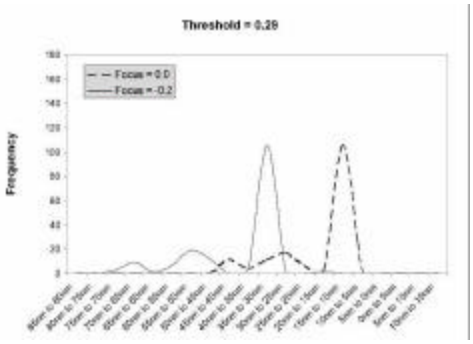


Figure 5.1: Layout Process Signature (Focus)

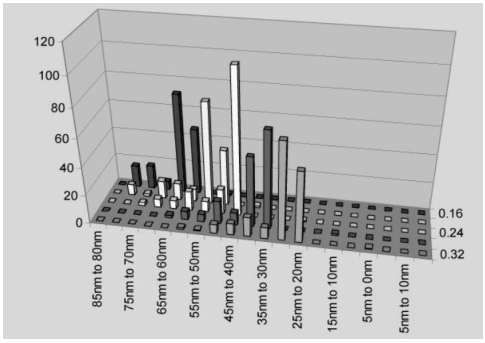


Figure 5.2: Layout Process Signature (Focus,Dose)

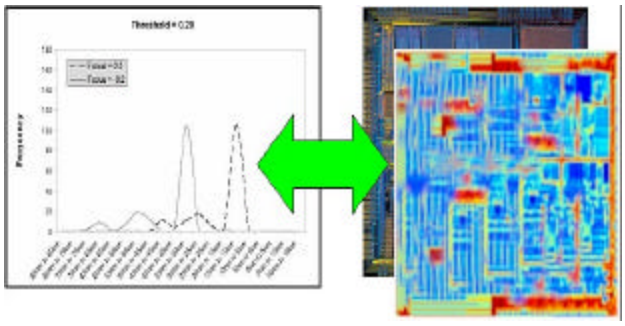

Figure 5.3: Layout Process Signature (Full-Chip Map)

## 5 Conclusions

Physical integration goals as defined by the International Technology Roadmap for Semiconductors, for 65 nm, 45 nm and below require manufacturability verification of Physical Layouts to supplement (at design time) traditional Design Rule Checks.
This paper has described the fundamental structure of a software building block to be used in such manufacturability applications. Three novel algorithms have also been presented for the extraction of quantifiable manufacturability metrics, either from DR's sets or from full chip layouts.
Challenges in the deployment of these tools in the design flow, lie in the intrinsic interdisciplinary nature of DFM tasks. Collaboration between chip designers and fabrication engineers will be an essential element of successfully manufactured designs. The potential reward for overcoming "cultural" engineering barriers will be provided by the viability of DFM, not only as a technical tool, but above all, as an economic alternative to costly (and continuously delayed) Next Generation Lithography tools.

## References

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