The X Architecture: Roadmap for Design for Manufacturing Methodology

Presentation to Electronic Design Processes
April 14, 2003

Ken Rygler, President
Rygler and Associates, Inc.

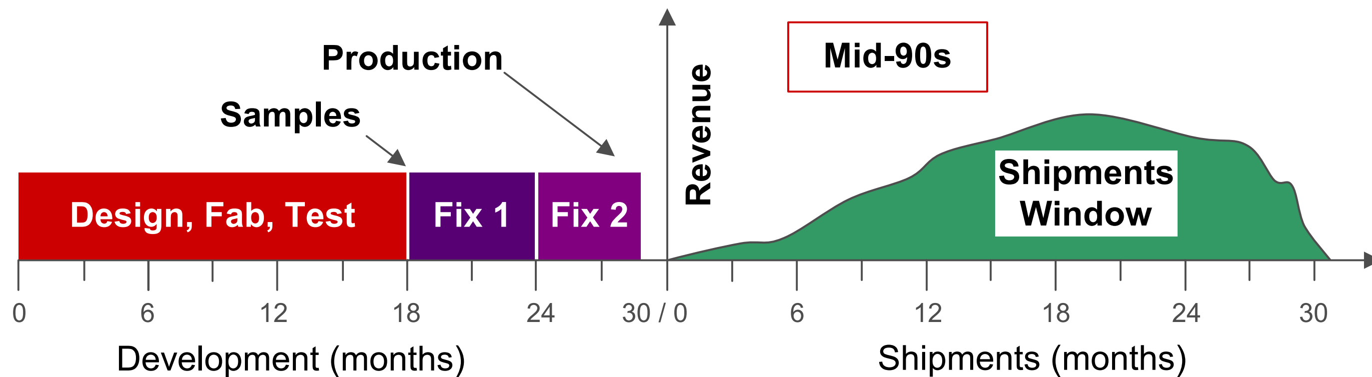
Agenda

- Background
- Industry Challenges
- X Architecture
- X Architecture Supply Chain - DFM
- Test Chip Results
- Summary

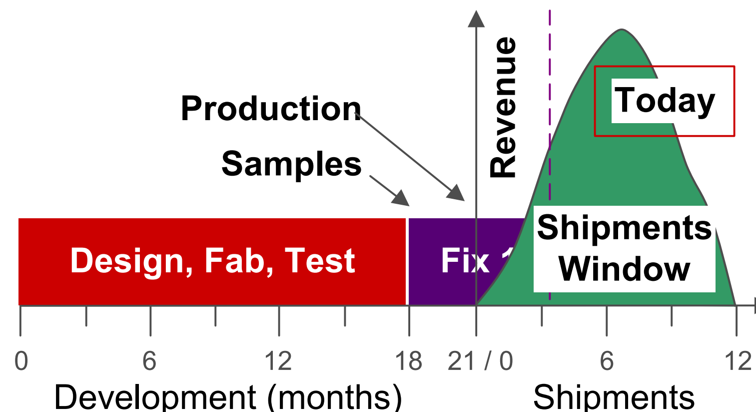
X Architecture DFM History

- Initial customer response positive
  - But can masks be made?
  - What about image fidelity? OPC? CDs?
- DuPont Photomasks produces first 180nm masks
- ASML prints 180nm silicon
- Numerical Technology implements OPC
- 130nm flow developed
- STM announces first test chips

Business Challenge:
There is No Market for a Second-to-Market



- **Mid-90s: 6 month late → ~31% earnings loss[1]**



- **Today: 3 months late = lose the market!**

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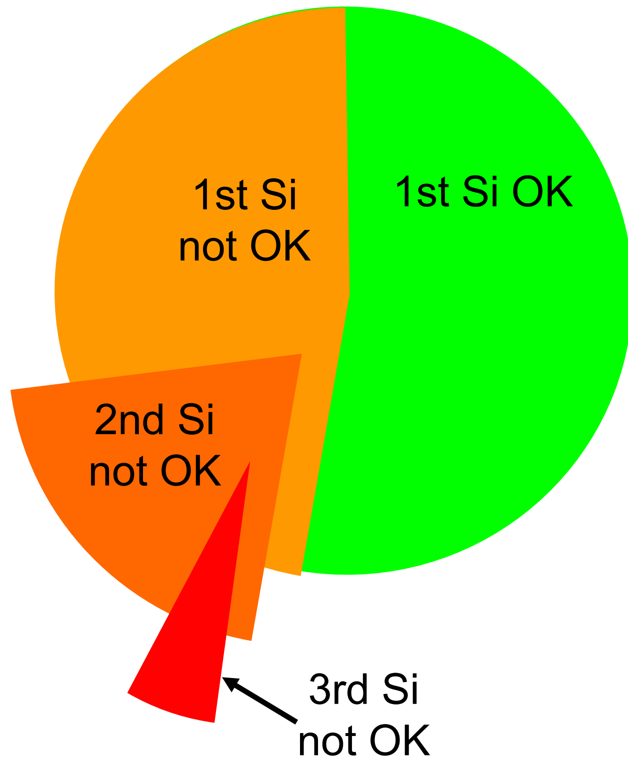
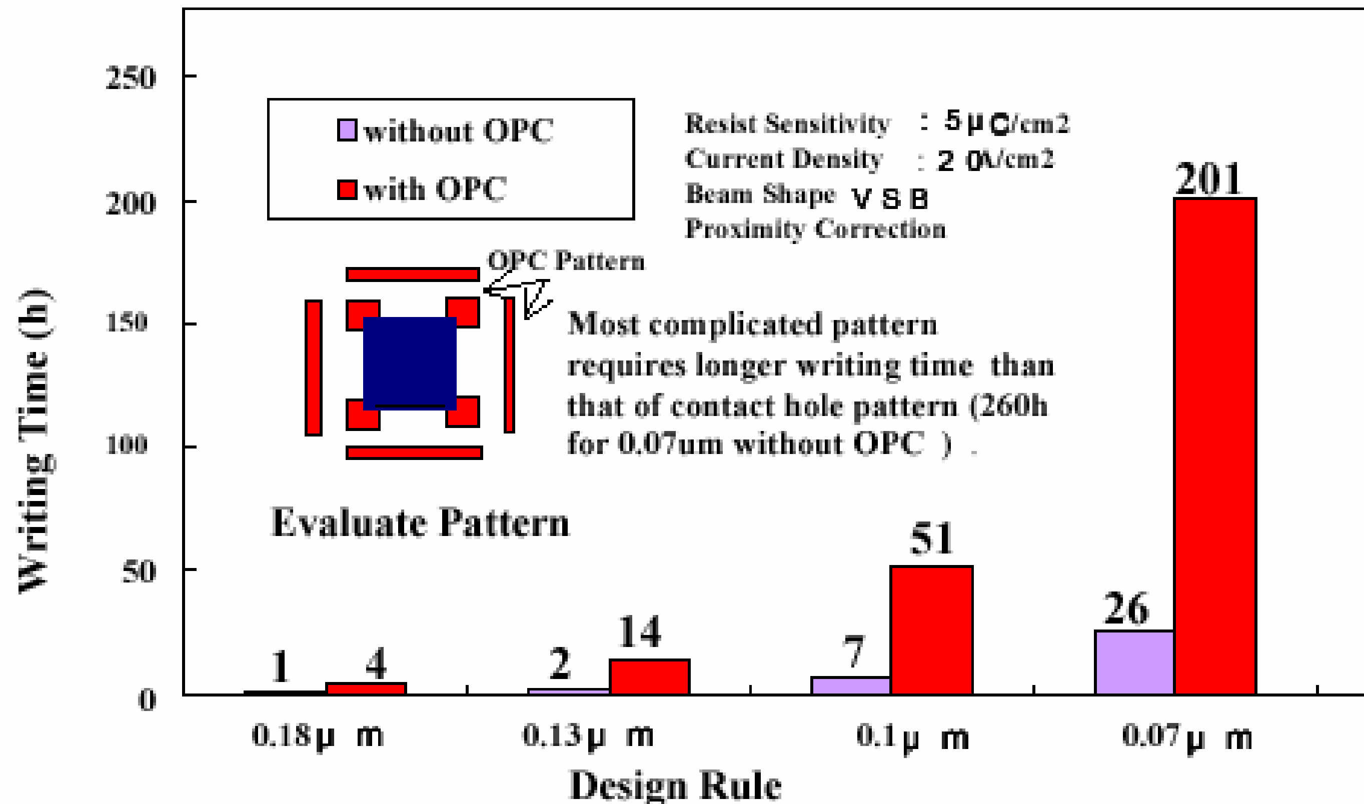
Silicon Failures Are Increasing



- 48% fail on first silicon[1]
- 20% still fail on second spin
- 5% still fail on third spin

1: Source: Collett International – 2000

OPC Driving Up Photomask Costs



Source : July 2001 Sematech EDA Workshop, Toshiba

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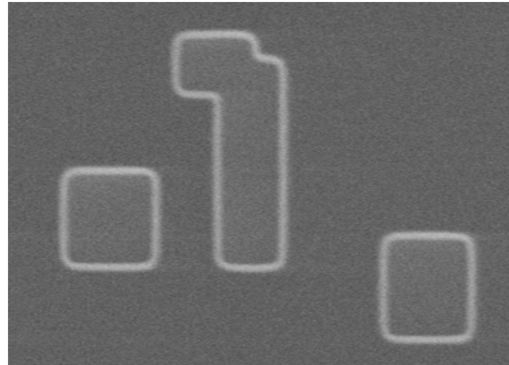
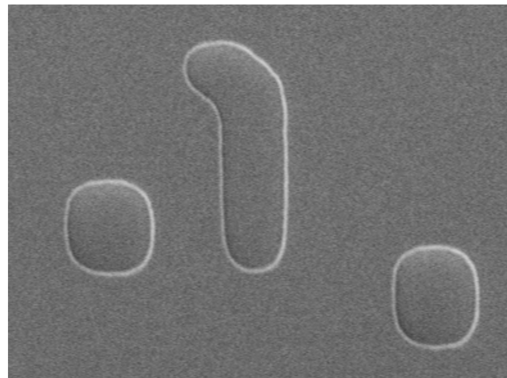
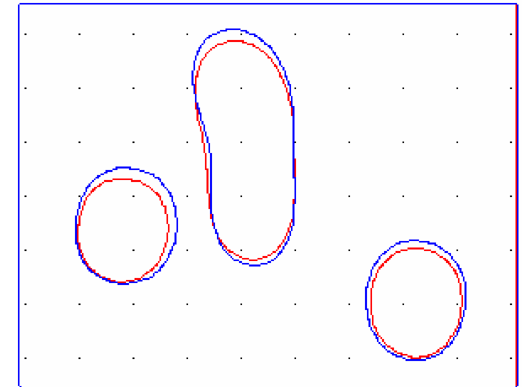
Photomask Patterning Impacts Mask Cost



Ebeam $$$$$



Laser $$$



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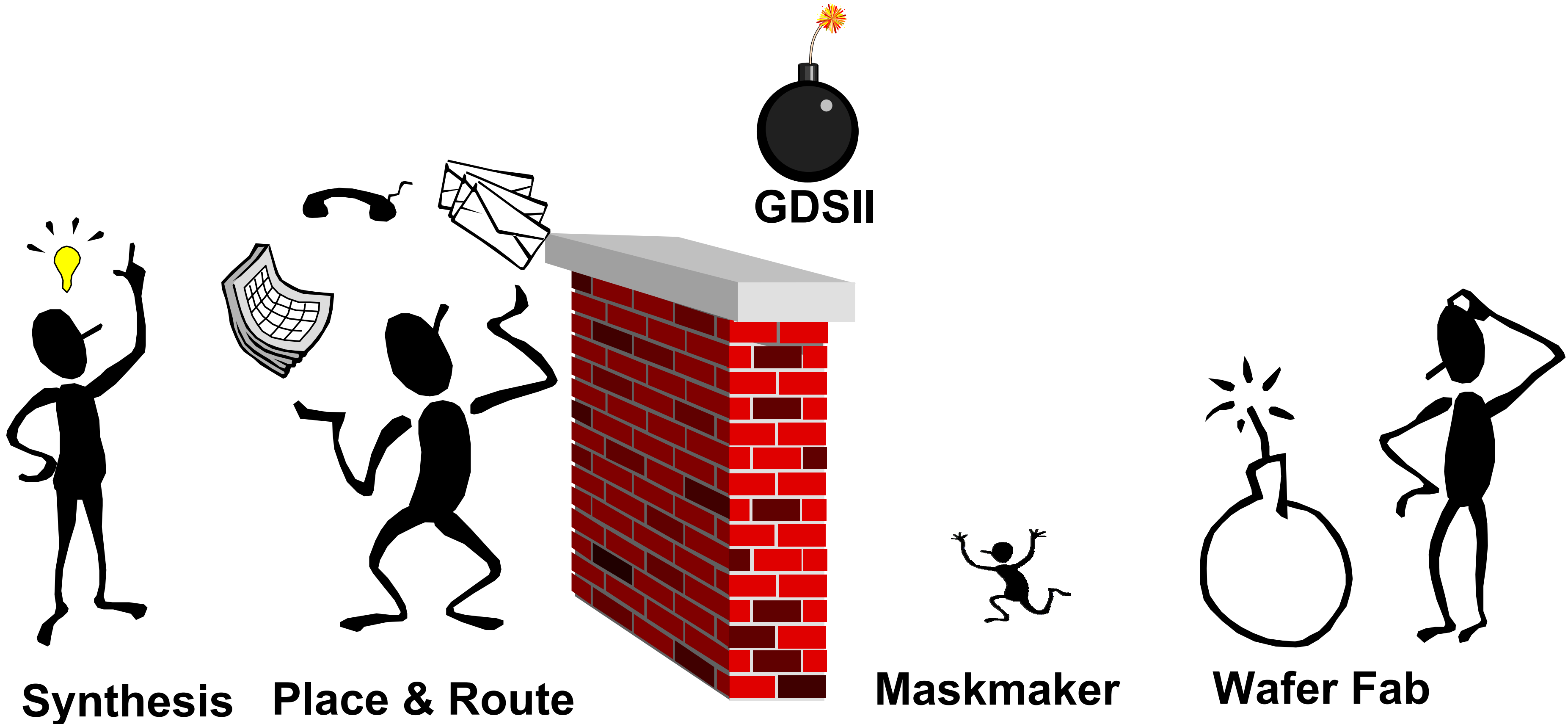
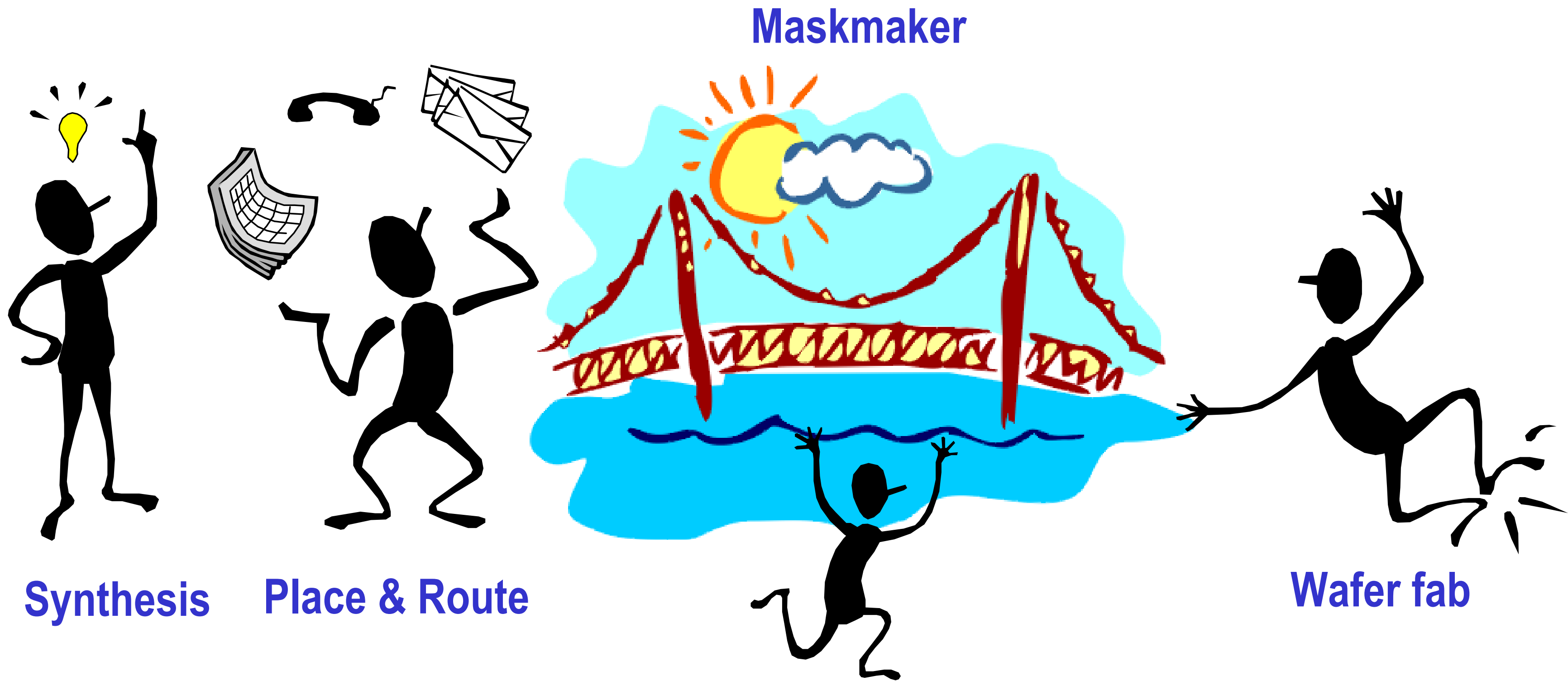
Source: DPI

IC Design and Manufacturing Process Circa 1995



IC Design and Manufacturing Process, ca 2000



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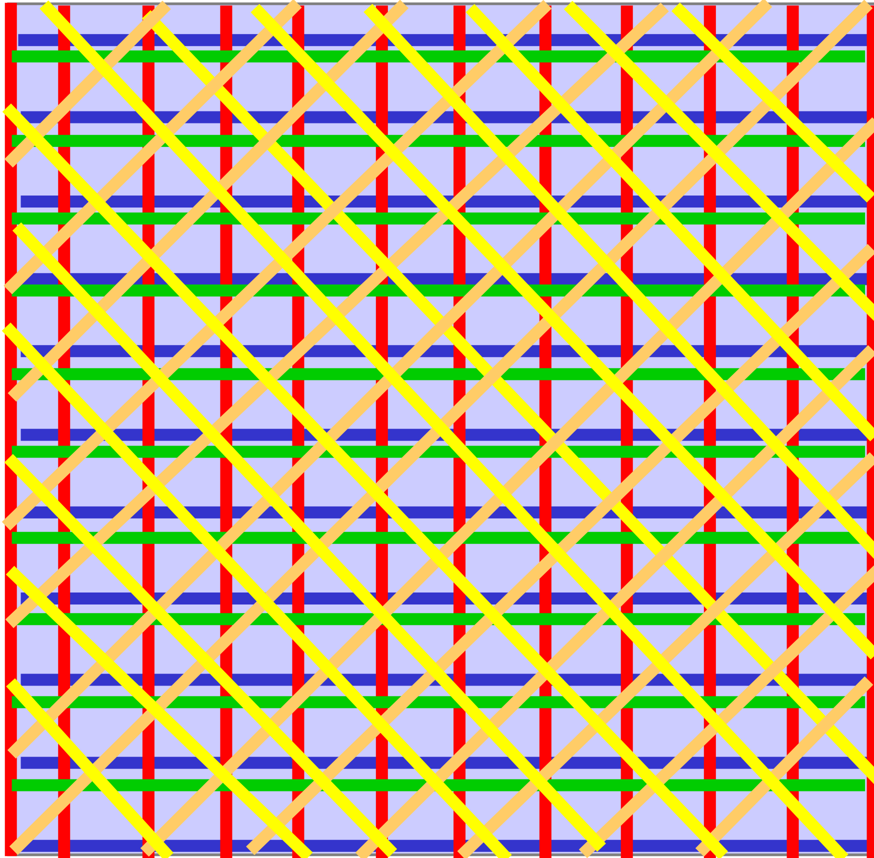
X Architecture:
Large-Scale and Small-Scale Diagonals

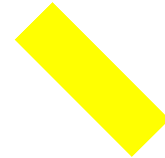
www.xinitiative.org

- 20+% less interconnect
- 30+% fewer vias

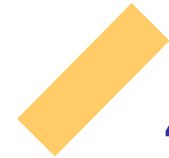
The X Architecture



Metal 5



Metal 4

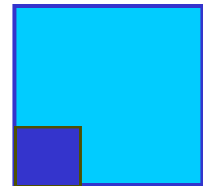


45°

Metal 3

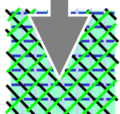
Metal 2

Metal 1



The X Architecture: Roadmap for Design for Manufacturability

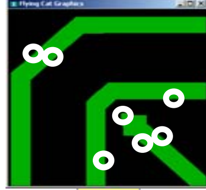
	First Availability	Expansion
Semiconductor IP Creation	✓ Confirm compatibility	
Design Implementation	✓ Physical Design ✓ Extraction	Test chips Design methodology
		OPC
Photomask Creation	✓Mask fracture & writing ✓Mask CD metrology ✓Mask inspection	Raster-based Vector-based Inspection
Chip Fabrication	✓ Design rules ✓ Lithography	Design rules Lithography



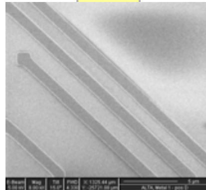
Technology nodes

130nm Mask-to-Wafer Supply Chain

Mask Data Prep



Mask Writing

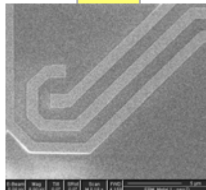


ETEC

An Applied Materials Company

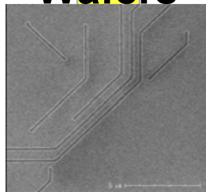
DuPont Photomasks, Inc.

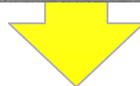
Mask Inspection



KLA Tencor

Wafers

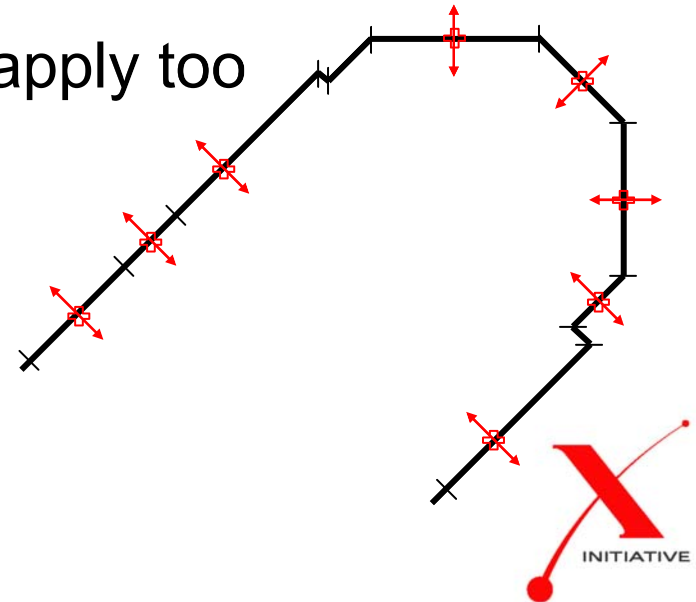




Nikon

Application of OPC on X Architecture 130nm Design

- Used Numerical iN-Tandem hybrid OPC
- Defined a “custom shape” for octagonal line end
  - Ensures limited data volume increase
  - Limits mask complexity and mask cost
  - Other OPC approaches would apply too aggressive OPC with possibly worse corrections



OPC Results

	Layer	Input (MB)	Output (MB)	Run Time (Hrs)	Estimated Production Run Time*
Bright Field	Metal 4	1.58	3.50	6.2	25 min
Dark Field			1.49	2.2	10 min
Bright Field	Metal 5	0.68	1.55	4.2	15 min
Dark Field			0.65	2.3	10 min

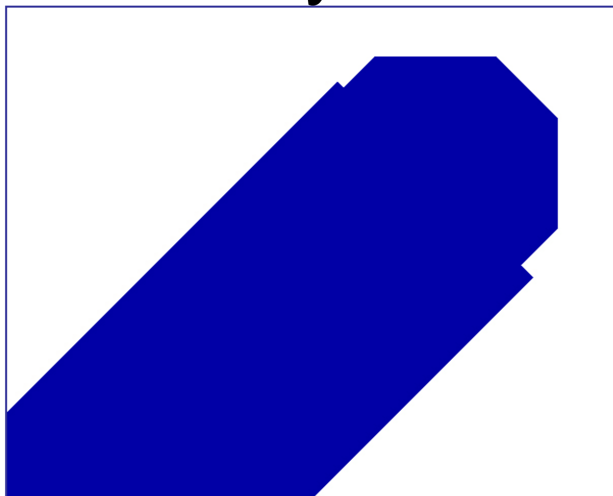
- Run times and output file sizes are well within normal ranges

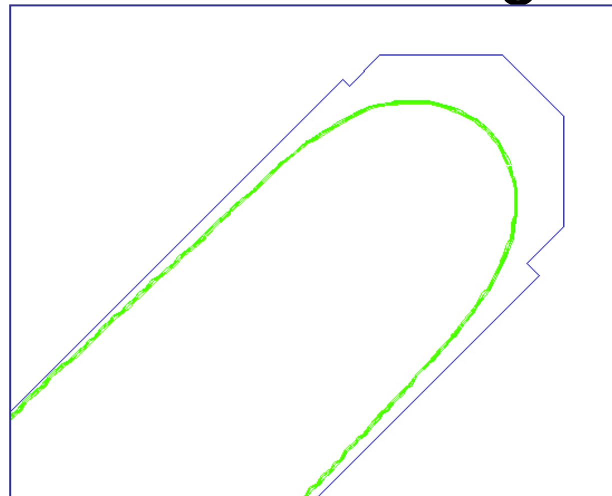
** Times are estimated based on a 20-CPU distributed processing production environment*

OPC Analysis: Octagonal Line Ends

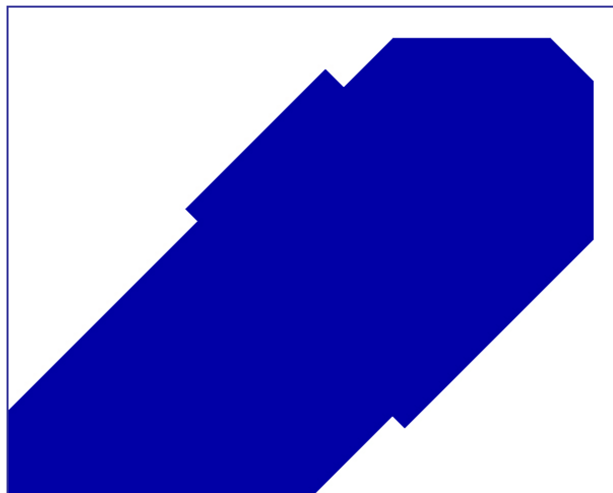
Layout | Silicon Image

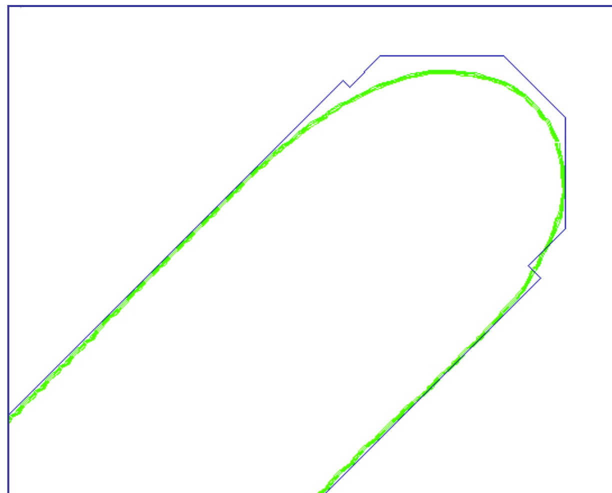
Original





After OPC





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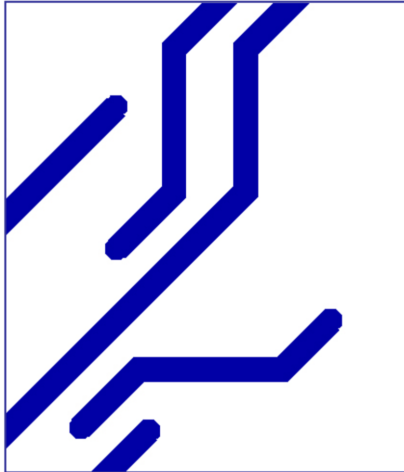
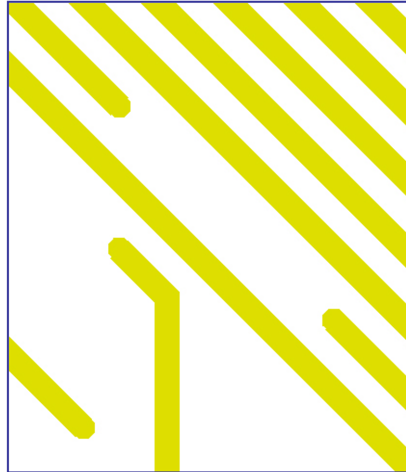
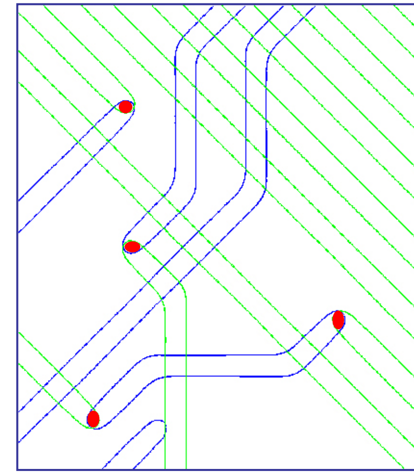
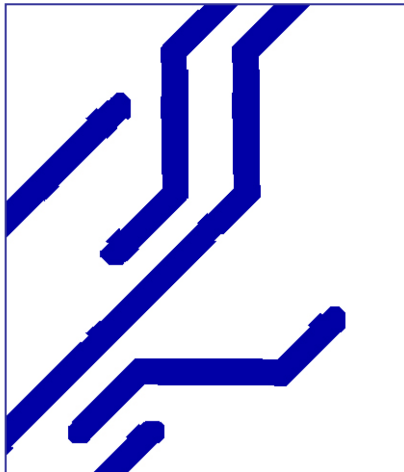
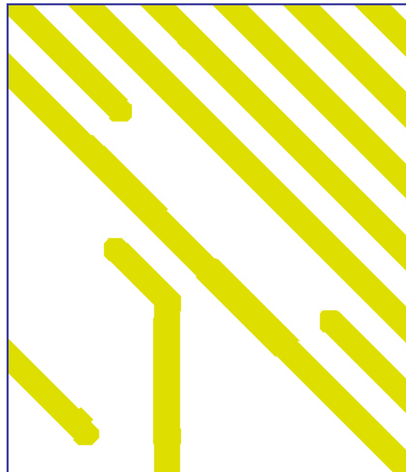
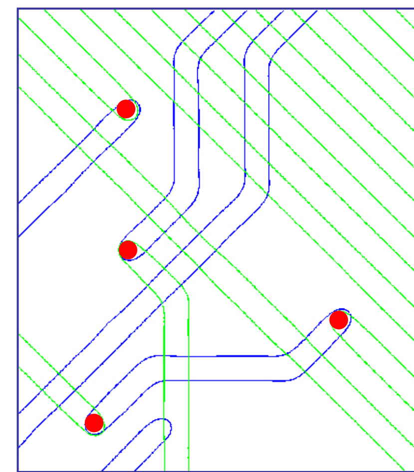
OPC Analysis: Via Enclosure

Layout | Silicon Image

Original

After OPC

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Numerical Technologies OPC Conclusions

- Feature sizes below 250nm require resolution enhancement techniques
- OPC is a requirement for manufacturing of X Architecture metal layers with octagonal features
- Appropriate OPC approach and tools can produce run times, and output sizes consistent with Manhattan designs
- Analyses confirm manufacturability and yield

DuPont Photomasks Produces First 130nm Masks

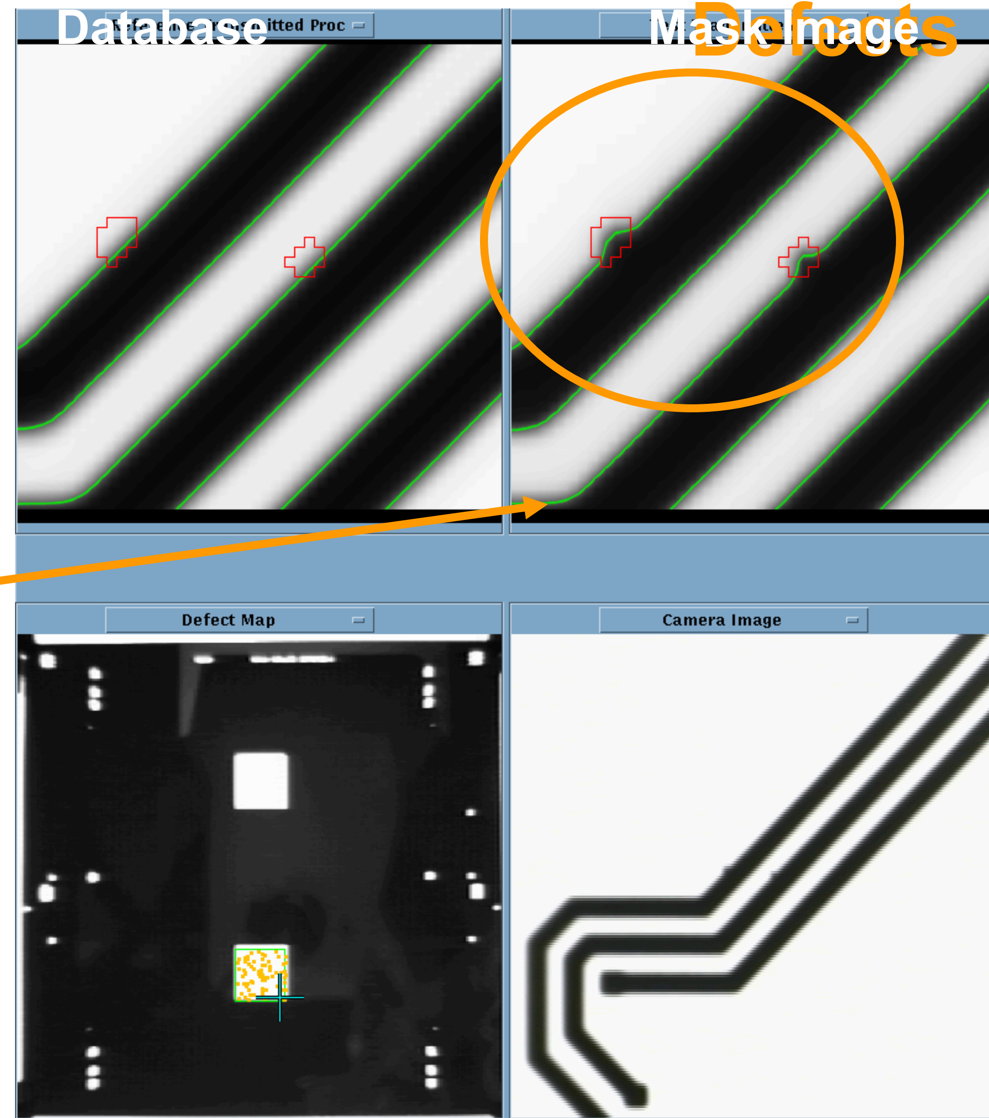
- **Results confirm manufacturability**:
  - Confirms Etec's ALTA 4000 raster laser writer
  - Confirms optimization of inspection

Process Step	Capability Indicator
Data fracture	Green
Data volume	Green
Write	Green
CD Measurement	Green
Defect Inspection	Green

KLA-Tencor TeraStar Inspection Conditions

- Two masks
  - 250nm DR mask
  - 130nm DR mask
- Inspection mode
  - Die-to-database
  - TeraStar standard algorithm – XPA
- Criteria: Monitor real and false defect counts

250nm DR Mask:
Examples of Real Defects and No False Defects



- Example of two contamination defects found on angle geometry edges.
- Note – no false defects at “elbows” as seen by previous generation inspection system.

KLA-Tencor Inspection Summary

The TeraStar F77 successfully inspects the 250nm DR and the 130nm X Architecture masks

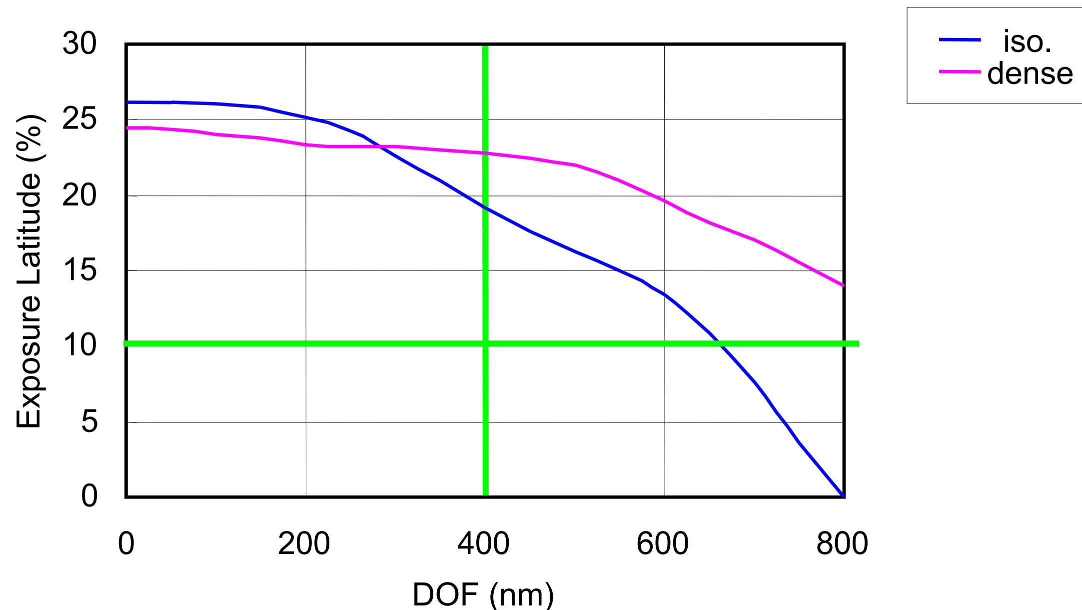
- 250nm DR mask - Most defects were large contamination – due to no pellicle
- 130nm DR mask – Handled the OPC, few or no false defects

Nikon Experimental Conditions

- Exposed wafers using DuPont Photomasks 130nm generation masks with X Architecture data (metal 4 and 5 layers)
- Nikon used its NSR-S205C DUV scanner to expose the wafers
  - For 220nm X, NA0.68 s0.85 2/3 annular / negative resist
- Criteria:
  - Process window
  - ΔCD

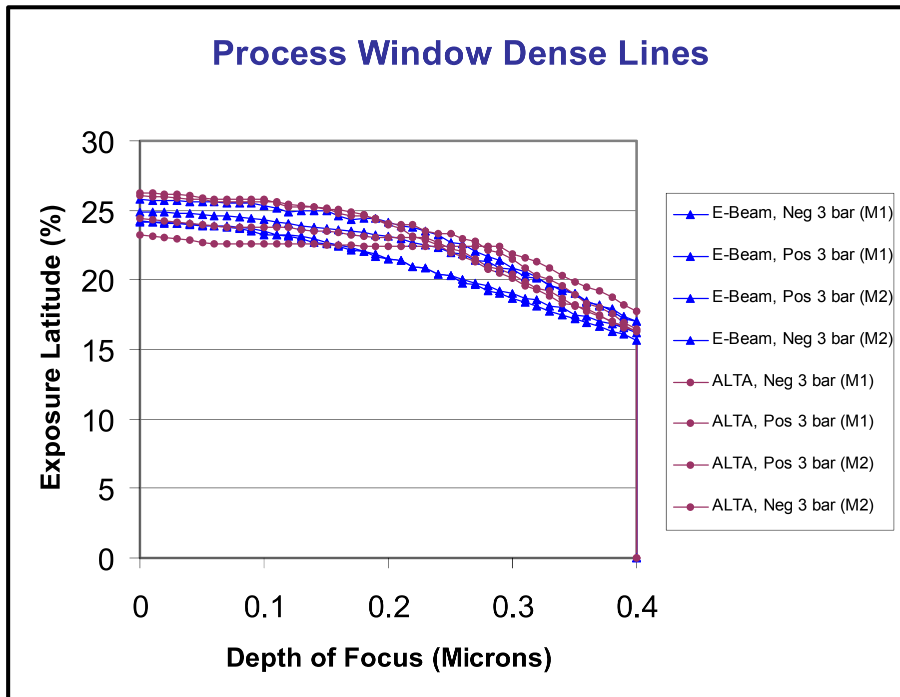
Process Window Results

- More than acceptable process latitude with X Architecture

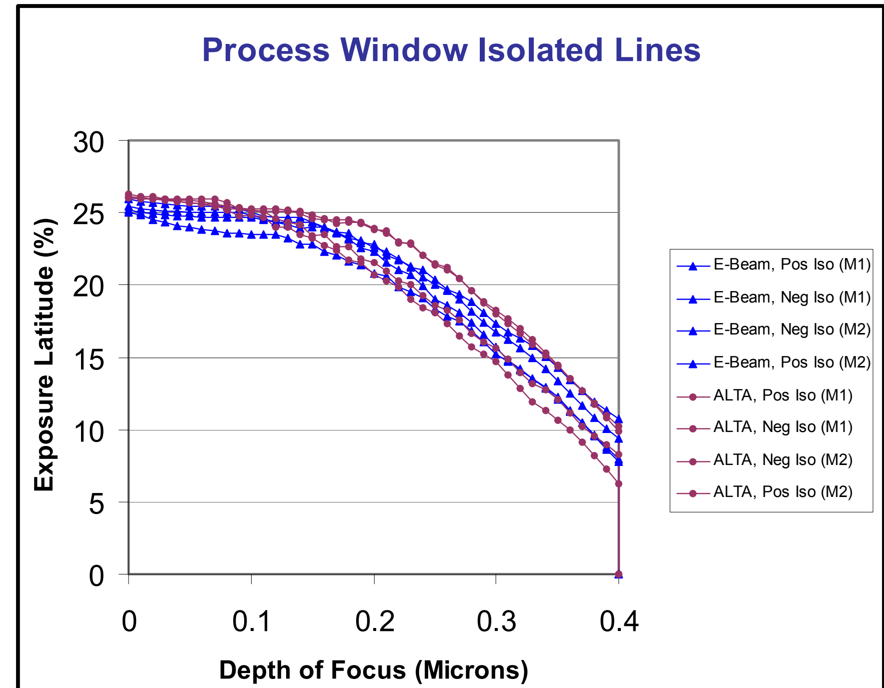


ASML X Wafers Results
E-Beam & ALTA comparison

X Technology - ebeam mask (Toshiba Machine EBM-3500)
X Technology - laser mask (Etec ALTA-3700)



L/S (3 Bar Structure - Dense Lines)

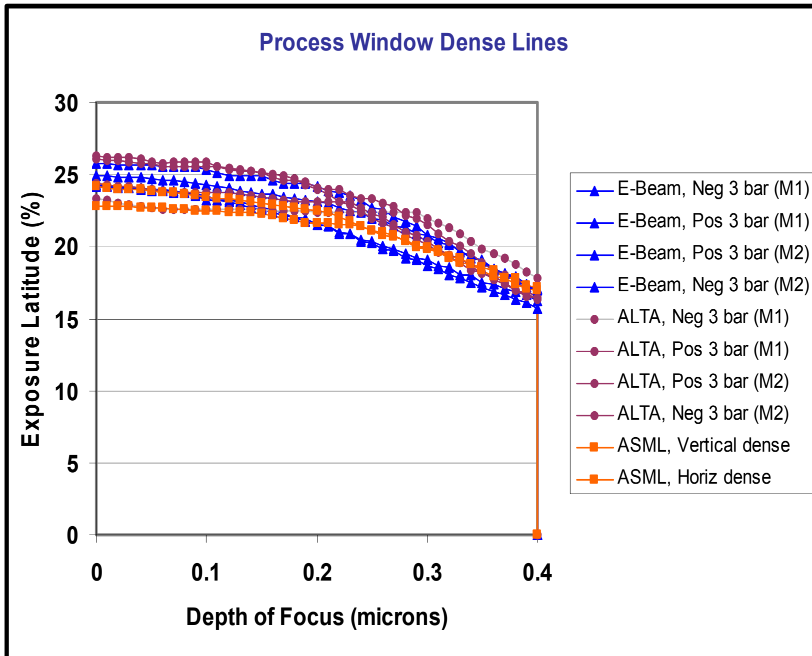


Isolated Lines

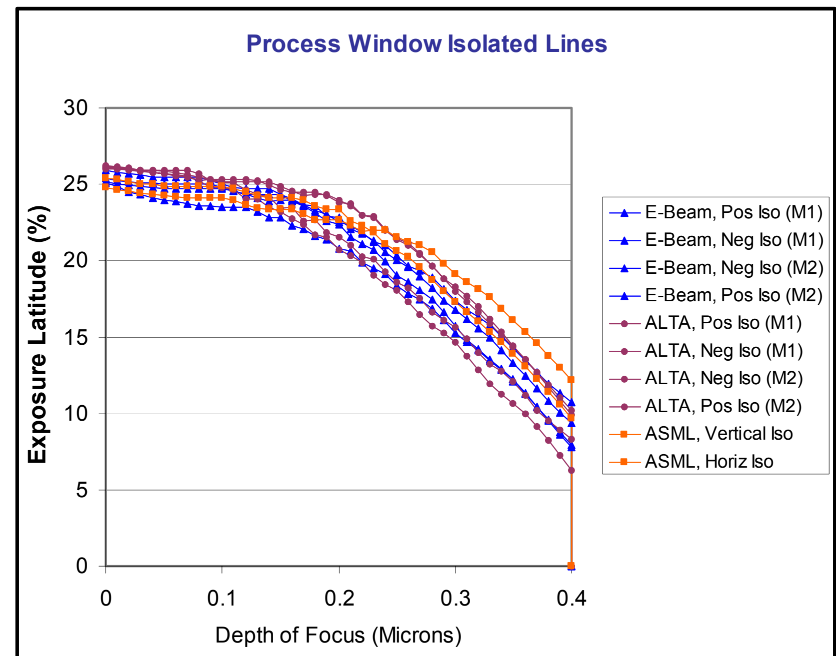
- No difference is observed comparing e-beam and laser generated X Technology masks

ASML X Wafers Results

Manhattan geometries
X Technology - ebeam mask (Toshiba Machine EBM-3500)
X Technology - laser mask (Etec ALTA-3700)



3 Bar Structure - Dense Lines

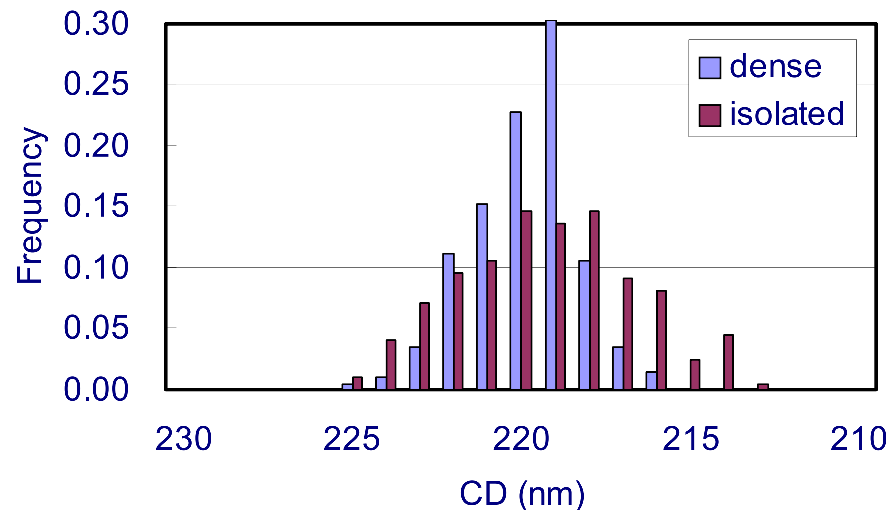


Isolated Lines

- No difference in manufacturability observed between Manhattan and X Technology non-critical dimension interconnect layers

CD Uniformity Results

- More than acceptable CD uniformity with X Architecture



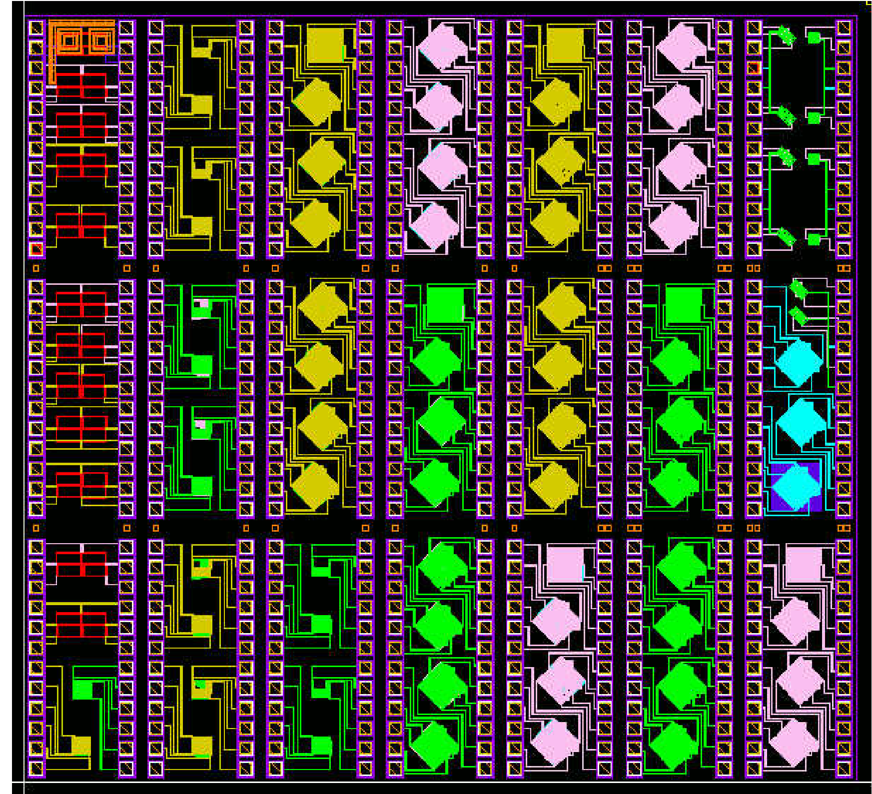
Dense 3s=4.6nm (2.1% of CD)
Iso. 3s=7.7nm (3.5% of CD)
Note: for wiring, up to +/-15% of CD is acceptable

Nikon's Conclusions:

- Using existing equipment and technology, the X Architecture is manufacturable today with sufficient process latitude and CD uniformity
- The X Architecture is a good additional test criteria for calibrating scanners for new technology nodes

X Architecture 130nm Testchip Results

- $25mm^2$ test chip with combs, serpentines, via chains at minimum pitch
  - all results OK on 59 dice!
  - We are pretty confident that we can manufacture X at minimum pitch in 130nm!
- Next test chip in 90nm soon



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The X Architecture: Roadmap for Design for Manufacturability

	First Availability	Expansion
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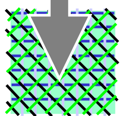
Chip Fabrication	✓ Design rules ✓ Lithography	✓ Design rules ✓ Lithography



Technology nodes

Summary

- X Initiative developed “soup to nuts” design-to-lithography flow to demonstrate manufacturability of diagonal routing
- Accumulated more than 30 members including leading semiconductor and photomask equipment suppliers, maskmakers, EDA companies, and semiconductor companies
- How can we leverage some of the lessons learned from this initiative to the broader DFM space?

IC Design and Manufacturing Process, ca 2005

Fast tapeouts, cheap masks, high yields