Communications 101 for EDA

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# 'Processes are for Beaurocrats!'

- 'Processes are just excuses used by beaurocrats to avoid doing real work!' -- Jason Jennings, from *Less is More*

  - *Oh well, he's just a journalist*

- Processeses and methodologies are, in truth, our 'corporate memory' for achieving consistent results

  - Thus, all businesses need them to varying degrees

  - They provide a recipe for Output=F(Input)

- The greater the dependencies and interactions, the more complex the resulting process

- IC design flow ependencies also demand complex communication among tools

Design Flow Methodology

- Lots of abstractions: Math, Event, Logic, Boolean, Physical, Polygon, Optical/Chemical (physics)

  - 80% / 20% rule favors front-end focus, but...

  - Attention returns to physical/physics challenges at each new node, must revise old methodologies

- Top-down intent meets bottoms-up physics at each level

  - Implementations (solutions) always bring bottoms-up constraints

  - Knowledge of intent useful (or critical) downstream

  - Need to pass information upstream, too
    - Is this just a "model"? What about dynamic dependencies?

Enabling Methodology Choices

- IC design and manufacturing methodologies are becoming inter-dependent
- Methodology choices are constrained by implementations

Enabling Technology

Realized Methodology

Next Challenge

Desired Methodology
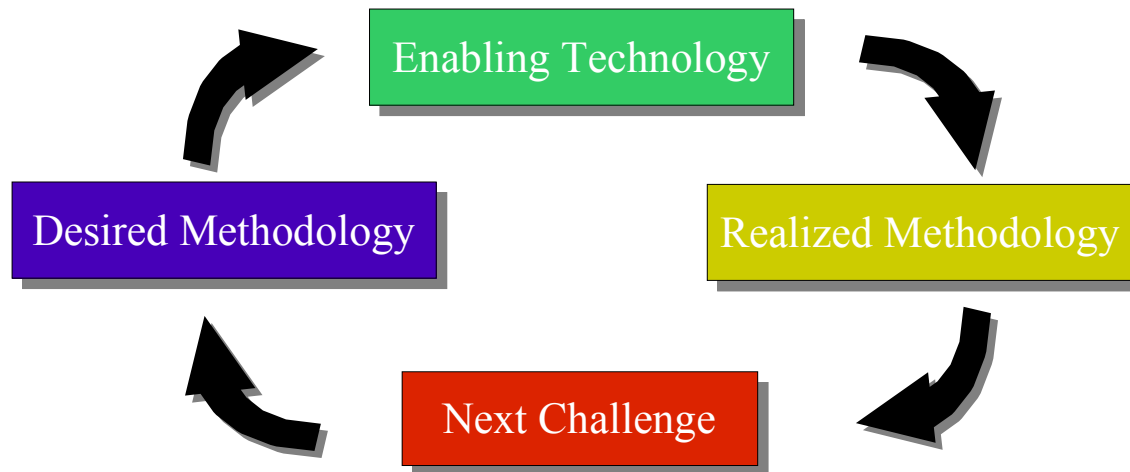
- The trick to enabling new IC flow methodology choices is better *communication* among the tools

130nm Frustrations Only the Beginning

> News

Trouble at 130-nm node causes finger pointing

By Stephan Ohr and Ron Wilson
EE Times
June 14, 2002 (5:33 p.m. EST)

What about 90nm??

(SNIP)

Some designers, meanwhile, voiced their frustration over bottlenecks in design flows and pointed a finger at EDA vendors. The design flows are broken, said users like John Szetela, manager for tools integration at Advanced Micro Devices Inc., and Hilton Kirk, manager of physical design at Philips Research Labs. "Late changes in the design flow are inevitable □ and the automated design flow is too slow to accommodate them," said Szetela. Point tools for analyzing postlayout parasitics □ IR drop, electromigration, antenna effects, signal integrity □ conflict with timing-analysis tools, he said.

(SNIP)

90nm: Chip Design At The Crossroads

- The challenges predicted for 90nm design are now upon us

  - Very compelling, and substantially worse than 130nm design*

- Many file formats have reached the breaking point

  - 2GB / 4GB file size limits on SPEF, SDF, LEF/DEF, GDSII,...

  - 32-bit no longer sufficient for large die area and small features

  - Total (SoC) chip design data >80GB @ 130nm (w/ current flows)
    - Predicted to exceed 200GB @ 90nm (w/ current flows)

- Co-dependent processing required among multiple concerns

  - No single supplier solves 100% of flow needs

- File format conversions already wasting too much time

  - Ex.: 110 min. for PDEF R/W with commercial layout tool*

  - Direct access is critical to avoid unacceptable project delays

Resolving Barriers in IC Design Flows

- Exploding Data Sizes:
    - Eliminate data redundancy
    - Smarter data structures
- Increasing Cycle Times
    - Avoid flow iterations
    - Faster access to required data
- Design Capacity, Performance Limitations
    - More efficient storage
    - Direct access to specific data
    - Best-of-breed tool algorithms

- **Co-dependent Processing Steps**
    - Fine-grained data interaction
    - Means for shared session control
- **Multi-Vendor Integration**
    - Common, extensible, high-bandwidth interface
- **File Format Interface Revisions**
    - Separate stable interface from evolving content

- What do tools need to communicate with each other?

    - Shared protocol

    - Shared semantics

    - Access to (only) desired data

    - Awareness of change to data

    - Persistence

- EDA has lacked a common 'language' for tools in flows to communicate... until now

- But wait, it's even more challenging!

    - Mask-level interdependencies with design now demand new methodologies that require communication across disciplines

What Makes This So Hard?

- Efficiency -- How to minimize access latency?

- Granularity
  - Design data sets are huge, multi-dimensional
  - Tool algorithm access needs varies widely, and are NP-complete

- Capacity – Indexing, compression w/ varying design data structures

- Robustness -- Represents data needed by current tool algorithms

- Concurrency -- Shared runtime memory access, synchronization

- Multi-Processing – Leverage parallel HW for big design tasks

- Flexibility – Adapts easily to new data requirements, custom tools

- Versioning – Everything must evolve but still retain interoperability

- Cross-disciplines – Different worlds and semantics make it harder

I. Single executable process (e.g. one big tool)

- (+) Shared memory, optimized

- (+) Direct data access

- (-) Fixed, rigid methodology

- (-) Lacks customization flexibility

- (-) Forces sequential processing
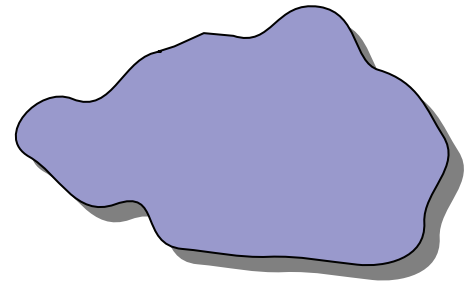
II. Multiple executables, direct MMAP sockets

- (+) Shared memory

- (+) Direct data access

- (+) Loads only algorithms / structures as required

- (-) Tool set compiled as single, fixed cluster

- (-) Cannot support distributed processing
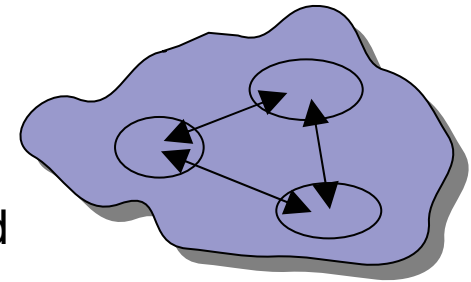
III. Multiple executables, defined protocol to common interface layer

- (+) Supports shared memory (and persistence)
- (+) Direct data access
- (+) Loads only algorithms / structures as required
- (+) Methodology and customization flexibility
- (+) Supports multi-threading, distributed processing
- (-) Interface implementations must be consistent
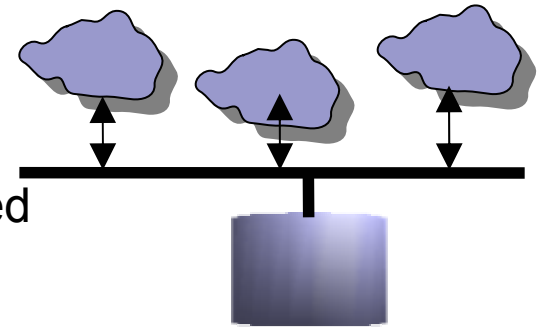
IV. Separate file formats between executables

- (+) Relatively simple to define
- (-) Poor performance on large data sets, repetitive steps
- (-) Very poor performance with coupled interaction
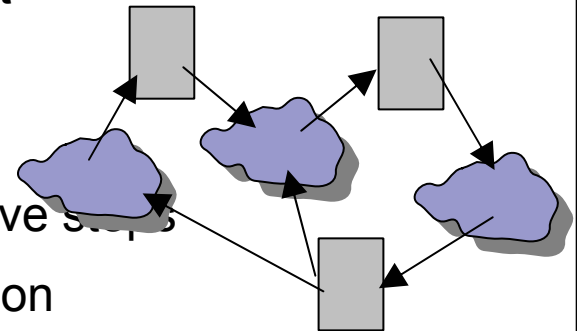
Process level integration

Design to Manufacturing Data Sharing

Multi-vendor integrated systems

Open Data API

— 2002

Single vendor integrated systems
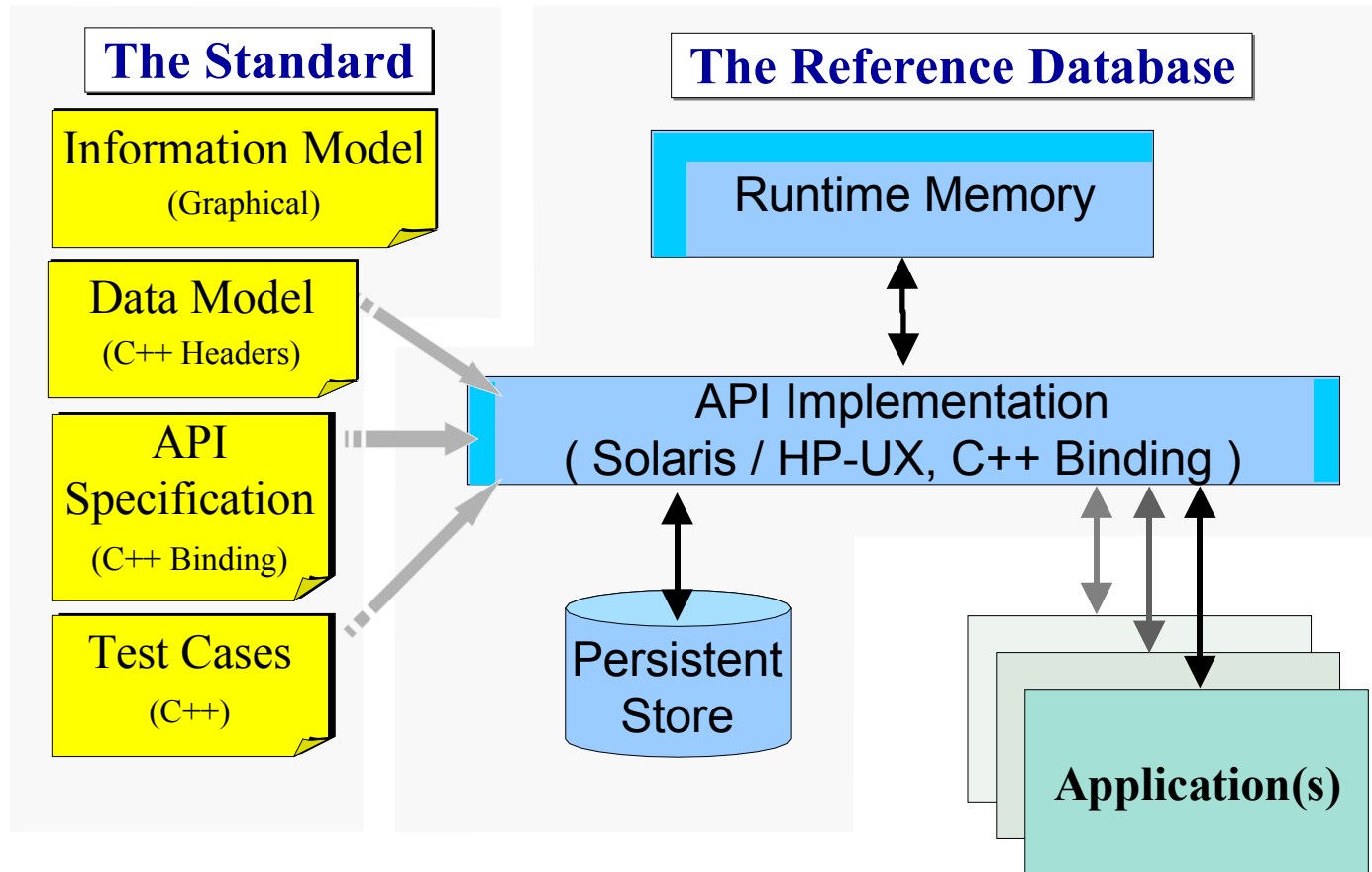
Proprietary Data APIs
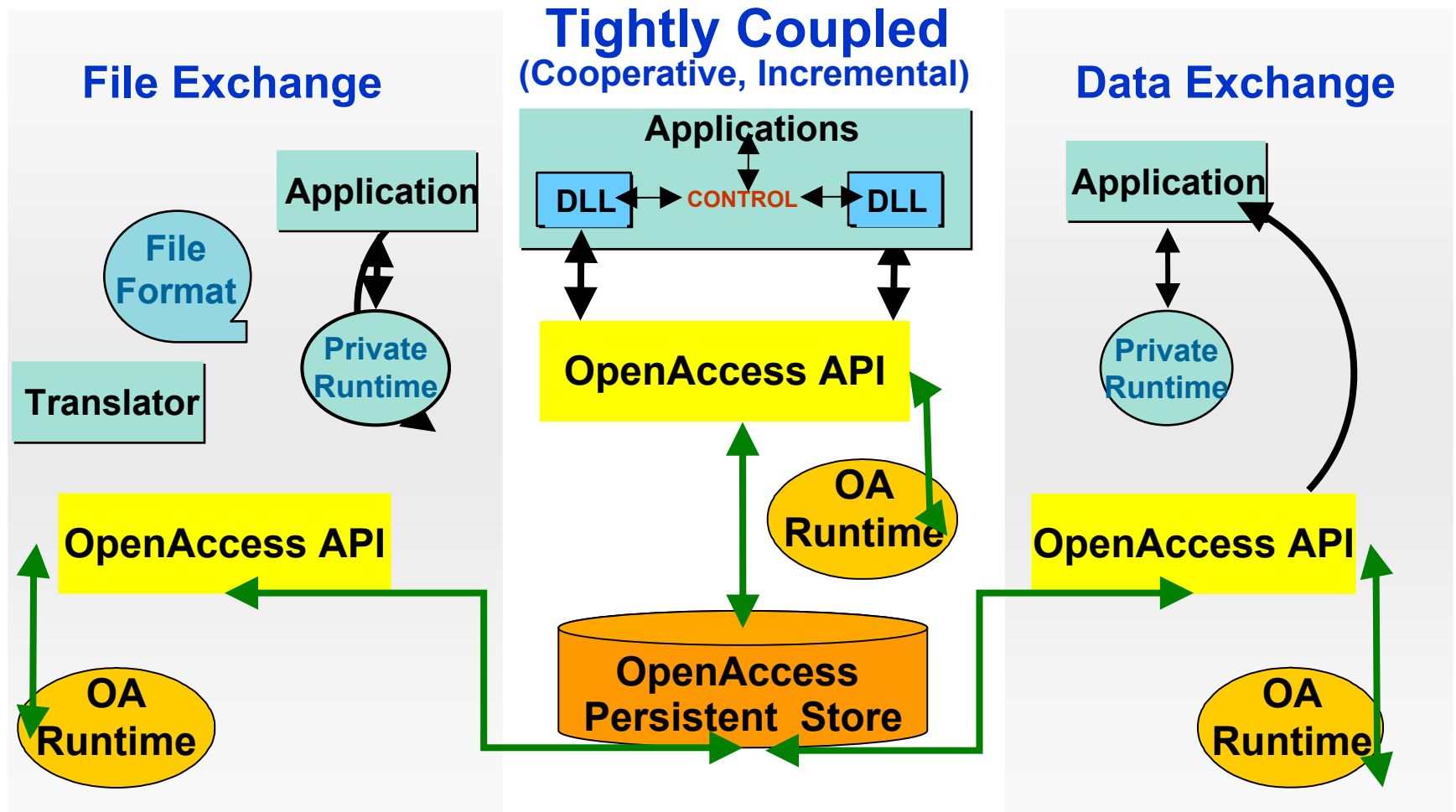
Loosely coupled systems

Open File Formats

Tool-Data Binding

Proprietary File Formats

Application Integration

Tightly Coupled
(Cooperative, Incremental)

File Exchange

Data Exchange

Applications

DLL ◄► CONTROL ◄► DLL

Application

File Format

Application

Private Runtime

Private Runtime

Translator

OpenAccess API

Application

OpenAccess API

OA Runtime

OpenAccess API

OA Runtime

OpenAccess Persistent Store

OA Runtime

OA Runtime

OpenAccess Process

Community

OpenAccess packages

Contributions Issues

Code Repository

OpenEDA.org
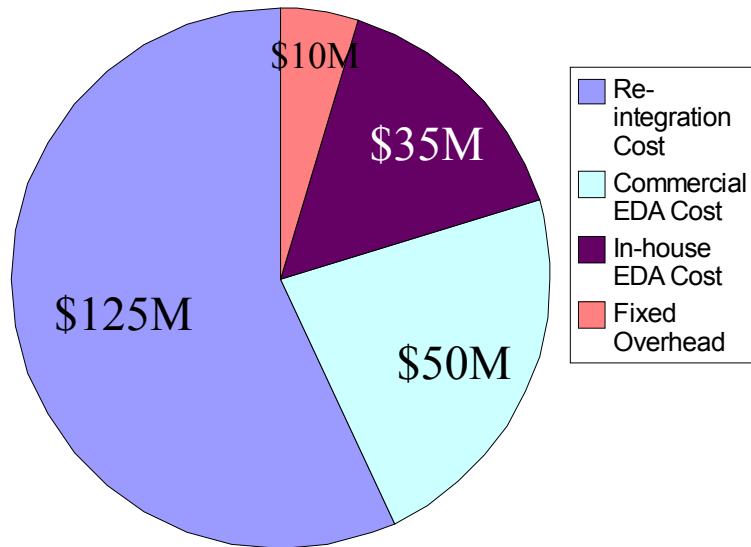
Issue Tracking System

Cadence or Contractor
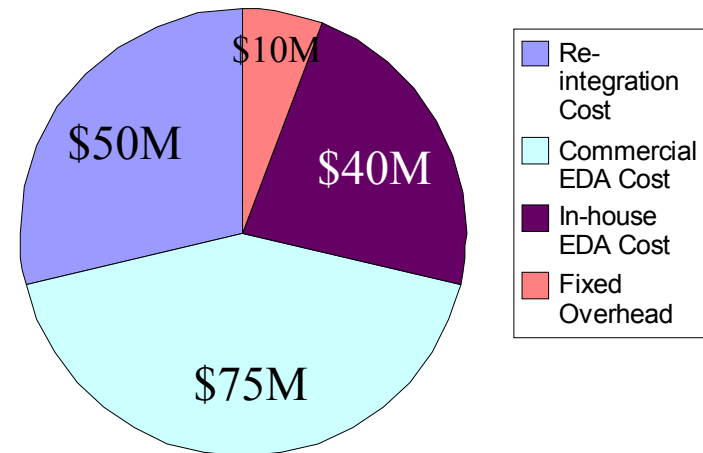
Change Team

Coalition

Improved Cost Efficiencies

- **Customers waste less on re-integration costs**
- **More potential for commercial EDA tool purchases**
- **Example: Corporate EDA budget of $220M**

Current Situation

$10M
$35M
$125M
$50M

Legend:
- Re-integration Cost
- Commercial EDA Cost
- In-house EDA Cost
- Fixed Overhead

Total: $220M

With OpenAccess

$10M
$50M
$40M
$75M

Legend:
- Re-integration Cost
- Commercial EDA Cost
- In-house EDA Cost
- Fixed Overhead

Total: $175M

Directions Ahead: OASIS, UDM

- Use of OPC / PSM compounding the data explosion problem

    - larger die area $\cap$ smaller features $\cap$ more accuracy $\cap$ RET

- IC mask costs rising out of control, threatens industry growth
- Advanced data handling for new mask tools (laser, e-beam)
- What's Needed:

    - Better data efficiency (OASIS ~ $1/10^{th}$ GDSII data size)

    - Higher bandwidth, direct access (OA)

    - Smarter data representations (OA)

    - Bi-directional design intent exchange (OA)

- Potential for $4B-$6B industry savings if solved (source: SEMI)
- SEMI has endorsed OpenAccess as their technology of choice

    - UDM = "Universal Data Model" (mask, test, yield improvement)

Mask Set Cost Escalation

- Mask cost is becoming a major impediment for low volume ASICs
  - At 90nm: $1.5M for typical mask set (up 85% over 130nm)
  - 65nm predictions are far worse...

$10M

$5M

$2M

$1M

$500K

180nm   130nm   90nm   65nm   40nm
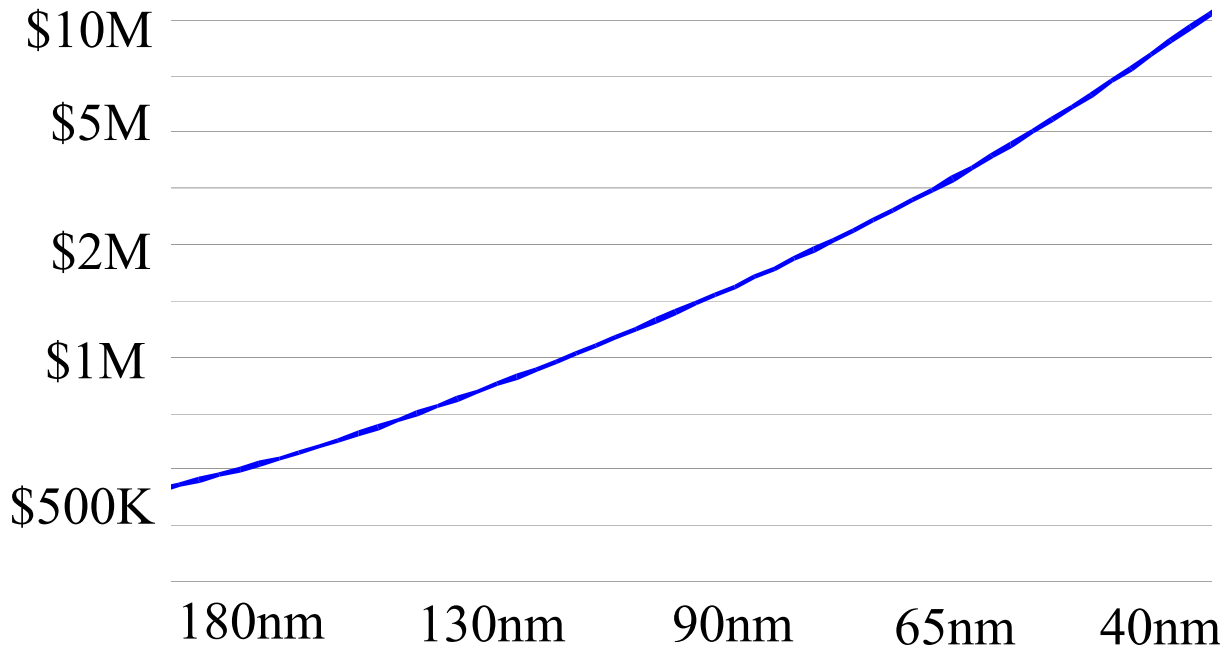
Mask Cost and Cycle Time Drivers
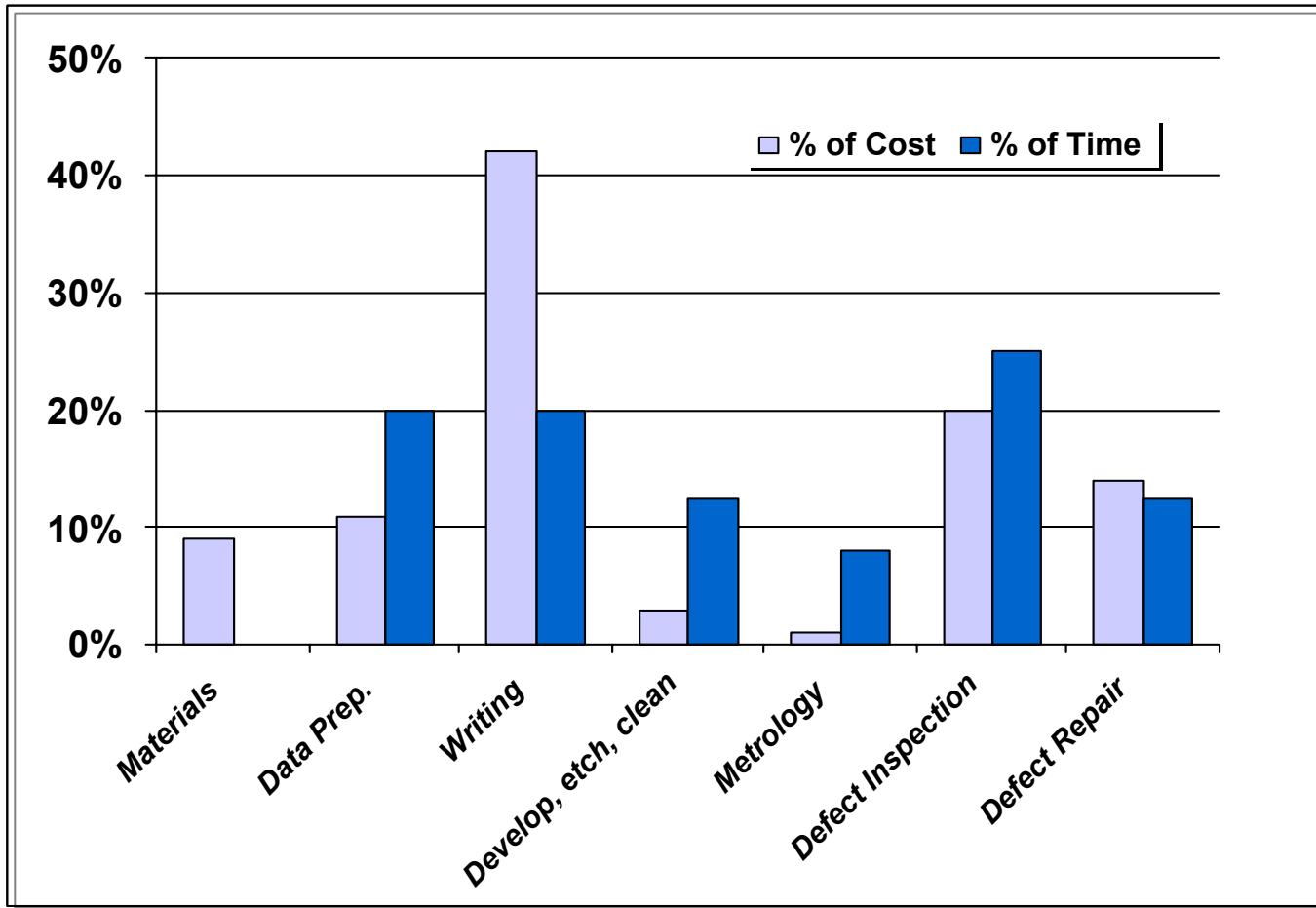
Source: TSMC

- [Exchange] file sizes too big

- [Exchange] file lacks extensibility/Adoption to change too slow

- Lack of manufacturing feedback to design

- Stream file looses too much design intent

- Ambiguous data model

- Lack of "Best Practices" Guide

- Too many [tool] formats

Source: SEMI EDA-Mask Taskforce 11/6/2001
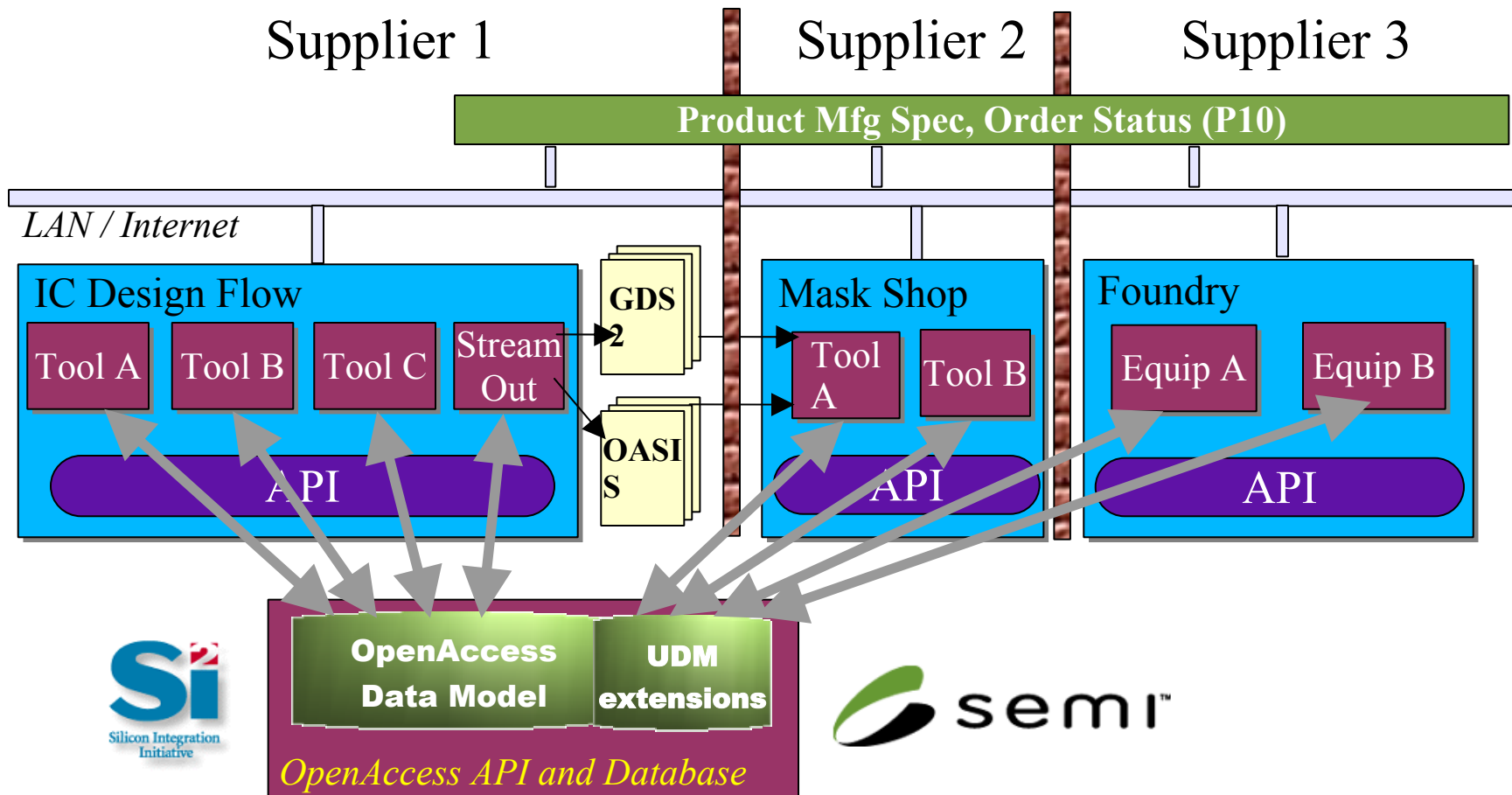
OpenAccess Features: Benefit to Manufacturing

Feature	Benefit
Full access to design intent	Aids diagnosis, analysis and repair
L/P hierarchies preserved	Reduces memory
Identification of OPC	Adds intelligent for analysis
Incremental R/W access	Very high-performance
Region selection	Reduces processing
Thread safe	Supports parallel processing
Fully extensible	Longevity
GDSII/OASIS translation	Eases migration, allows coexistence
Community source model	Controlled by all partners but without dependence on any

SEMI/Si2 Join Forces To Realize OA-UDM

Supplier 1

Supplier 2

Supplier 3

Product Mfg Spec, Order Status (P10)

LAN / Internet

IC Design Flow

Tool A   Tool B   Tool C   Stream Out

GDS 2

OASIS

API

Mask Shop

Tool A   Tool B

API

Foundry

Equip A   Equip B

API

OpenAccess Data Model   **UDM extensions**

OpenAccess API and Database

semi

EDA Standards: License Model Comparison

Classification of Standard	Rationale	Access		Distribution		Control	
		Rights	**Restrictions**	**Rights**	**Restrictions**	**Rights**	**Restrictions**
Open Source	Allow freely derived works, rapid evolution	Free, open use of source or binary code	Unrestricted access to source (1)	Source or binary, all versions of all changes	Changed source must be available, and allow derived works (1)	None	Undefined
Open Evolution ("Open Community")	As above, plus shared control process ensuring stable, converged evolution of standard	As above, with single public source download site	Unrestricted, royalty-free access to source (2)	Binary, including bug fixes and incorporated API changes	For distribution, modified source must be contributed within 30 days (2)	Elected change team with equal voting rights (2)	No single company can control evolution of standard (2)

(1) see opensource.org for complete description

(2) see openeda.org for complete description

Si2 Mission

Achieve industry adoption of collaborative technology and services that deliver higher levels of silicon design integration, enabling compelling advantages for our members through reduced costs, faster time to market, and improved IC design capability.

50% Semiconductor

29% Commercial
EDA Vendors

21% Electronic
Equip. Design

Our focus is on the **implementation** of *collaborative solutions*

Summary

- Methodology + new technology drives improved IC flows
- Improved tool communication is required for new methodologies
- Common, open API architecture addresses both performance and flexibility needs
- OpenAccess is the *only* open source API standard / database
- Si2 and SEMI are partnering to tear down the design-mfg 'wall'
- Now is the time to actively support OA and OA-UDM
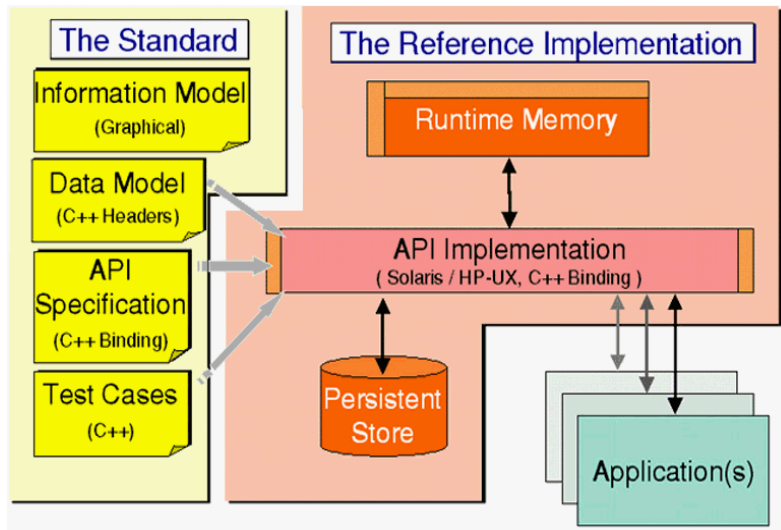
OpenAccess: A New Era in IC Design Has Begun