A Revolutionary Solution for Unified RF System and Circuit Design

James Spoto
Applied Wave Research, 1960 E Grand Ave Suite 430, El Segundo, Ca 90245

Abstract

In the intensely competitive mobile communications business, product time-to-market and profit margin pressures are increasingly acute. Often driving product delivery and costs is the RF system. The RF system is typically plagued with delivery delays and costly rework largely due to inefficient methodologies that segregate the RF system and circuit design process.

To overcome the limitations of this segregated approach, a unified RF systems and circuit design solution is introduced. Applied Wave Research's (AWR) Microwave Office 2002 and Visual System Simulator (VSS) provide RF designers an environment to achieve maximum performance and productivity. This paper describes the solution and its architecture. An application example is also presented.

1 Introduction

The diversity and complexity of wireless communication systems have made the separate specification of RF circuit blocks inadequate. Effective design of RF circuit blocks requires an awareness and understanding of their complex interactions in the context of the entire system at all level of abstraction. Within this context, designers must also be able to respond quickly to the rapid changes of mobile communication applications. The incessant demands of the this business i.e. the need to supply new and more sophisticated hardware to the marketplace with increasingly shorter market windows, mandate a truly unified and interactive RF system and circuit design solution.

The solution should facilitate near real-time monitoring of the impact and interplay of system, circuit and device design requirements and specifications at all levels based upon multiple supplier cellular design libraries. This paper describes a method and EDA solution for studying the interaction between levels and the trade-off of various system specifications, circuit topologies, device technologies and architectures.

2 The Traditional Approach

The translation of system concepts to circuit implementation has been largely a two level disparate process consisting of:

- System level design which is essentially the study of product architectures and their trade-offs using system level programs such as Matlab and SystemView. These tools offer a wide variety of high-level functional blocks enabling the simulation of complex communication systems.
- Circuit level design that is the construction of transistor and passive component schematics and the selection and sizing of their values. Circuit designers commonly use programs like Spice for time domain analysis and often use tools such as Cadence's SpectreRF, Agilent ADS and AWR MWOffice to simulate RF and distributed effects.

This approach lacks linkages between the system and circuit level with little connection between the implemented functional block circuit and its system model descriptions. This creates a serious bottleneck to studying the interaction between the system requirements and circuit level implementations.

3 A Unified Approach

To provide contemporary RF designers with an accurate and fast RF-system simulation, one can construct non-linear behavioral models of the circuit level components using harmonic balance techniques and import them into the system simulation environment. Using this approach, the impact on system performance factors (i.e. Bit-error-rates, power-spectral growth, symbol constellation uncertainty and eye-diagram aperture) as a consequence of RF circuit effects and impairments can be realized. These effects include:

- AM-AM, AM-PM characteristics of power amplifiers
- Frequency dependent feature of power amplifiers when they are excited by broadband signals
- Characteristics of low/band/high pass filters
- VCO's & their phase noise
- Mixer distortions

Figure 1 illustrates this process. The amplifier is shown both at the circuit level as a schematic and block level as a system component in a communication channel.

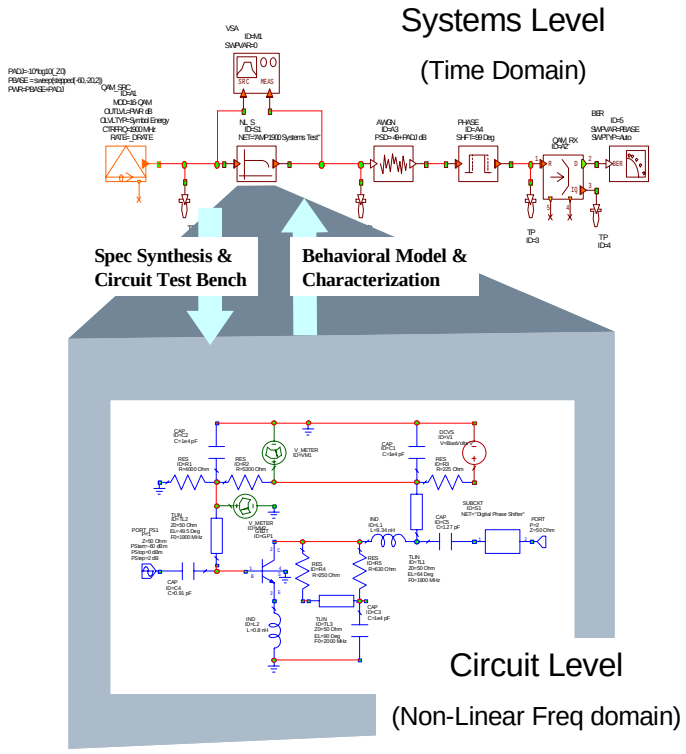

Figure 1 – RF system design hierarchy. The amplifier in the communication systems block diagram is expanded to its transistor circuit level schematic. The linkage between system and circuit tools has been poor until now.

Extracting systems level non-linear behavioral models from harmonic balance, circuit level simulation or measured results is not new. The concept has been around for years. The value of the method for improving the understanding of a system's performance in the presence of non-ideal RF impairments is presented in a recent paper by Krikorian and Goldstein [2]. In this paper, the authors describe a lengthy design flow connecting disparate tools with intermediate model/measurement data files in a non-real-time process.

What is new and has the potential to revolutionize RF system design is the implementation of this model creation and simulation as a real-time process within a unified system and circuit design environment. Such a solution offers the RF circuit and/or system designer an ability to understand, visualize and even optimize the impact of changes in circuit design parameters on systems level performance as never before possible.

4 Design System Architecture

Shown in Figure 2 is a simple view of the traditional EDA system structure. These systems are a union of individual tools (shown here are schematic and layout editors as well as simulator waveform output), each with their own database coupled by netlist, translators and data files. In many cases, each tool has its own disjoint user-interface. The overhead and redundancy of this form of integration makes tool interaction slow and lethargic i.e. much more a batch rather than a real-time process.

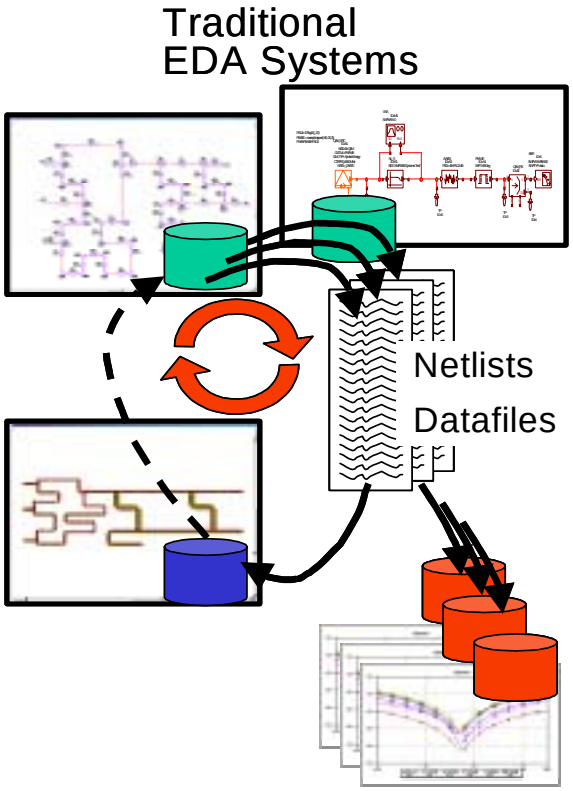

Figure 2 – Traditional EDA systems are an integration of heterogeneous tools with different databases. Tool interaction is accomplished through time-consuming and error prone netlists and translators.

What enables the real-time solution highlighted in this paper is a novel approach to integrating and presenting EDA tools in an intuitive and unified way, based upon:

1. A object-oriented design system architecture built from the ground up on a single database for modular, incremental and interactive RF tool integration and analysis.

2. High performance data-driven system and harmonic balance circuit simulators designed for incremental and interactive operation using

Microsoft COM compliant interfaces.

To contrast the traditional EDA structure, Figure 3 depicts our modern design system architecture.

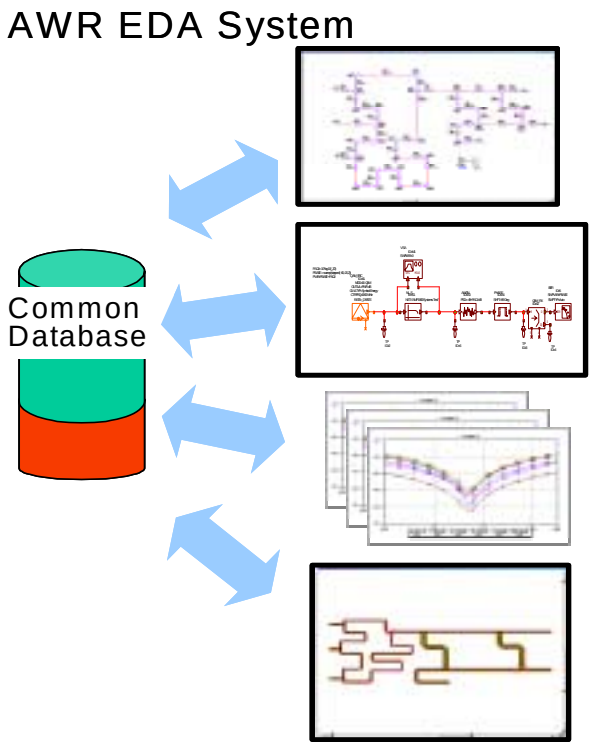

Figure 3 – The tools in the AWR solution all operate on the same data structure. When a property on the schematic or polygon in the layout is changed, all corresponding representations are updated and the simulators rerun and results redisplayed.

With AWR's solution, the EDA tools (schematic and layout editors, as well as simulators and waveform viewers,..) all write and read to and from the same database. Also, the design components and simulation engines are integrated as objects that inherit and process changes incrementally. So when a schematic property or layout polygon is changed or tuned, only those representations dependent upon the change are updated, simulators run (if required) and graphical waveform results refreshed immediately without explicit command entry. Shown in Figure 4 is an object diagram illustrating this event-driven dependency process. The parameter "a" change initiates the running of 2 simulators X and Y, and ultimately impacts the graphical output of simulator Y results, whereas, a change of parameter "x" only initiates and impacts Simulator Y and its graphical output.

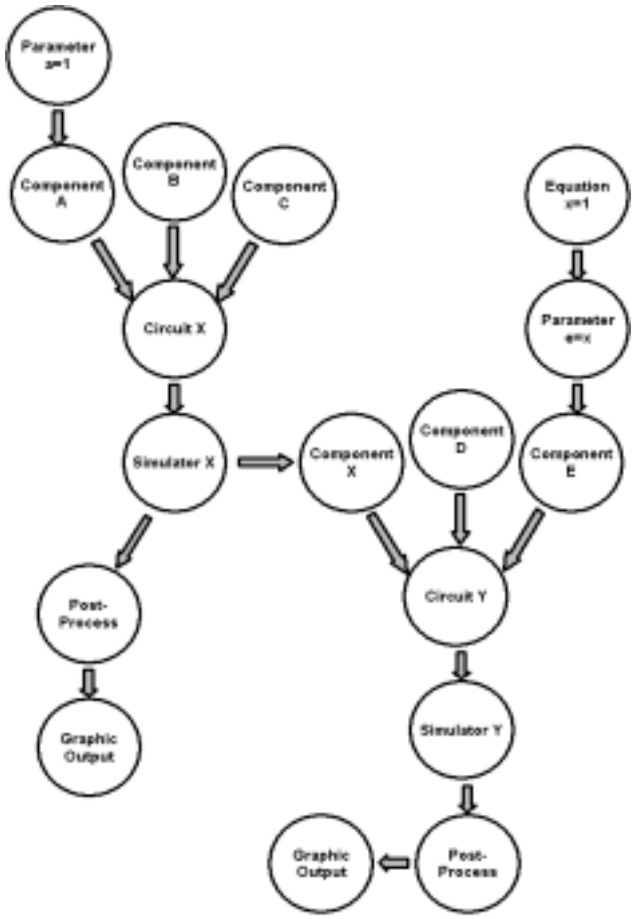

Figure 4 – In much the same way Excel spreadsheets work, property values are updated, simulators run and analysis results are refreshed selectively when a parameter they depend upon is changed. This updating process is implicit and requires no manual intervention to initiate.

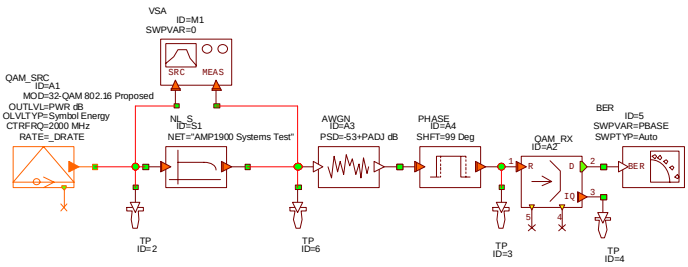

Figure 5 – A 2GHz 802.16 amplifier test bench.

5 Examples

To demonstrate the utility of our solution, we constructed the simple system block diagram shown in Figure 5.

The system is excited by the proposed standard IEEE 802.16 2GHz 32 QAM signal source as the input to a power amplifier. The amplifier, in turn, feeds a white Gaussian noise channel into a phase-shifter block that is finally terminated by a QAM receiver. The receiver is intelligent enough to adopt the 32 QAM characteristics of the signal source.

There are 4 test points defined in the signal chain and 2 measurement blocks are attached. One measurement block, the Vector Signal Analyzer, is strapped across the amplifier behavioral model to measure its AM-AM and AM-PM characteristics at the systems level. The other measurement device is a Bit or Symbol Error Rate (SER).

Figure 6 displays the power amplifier at the transistor level. A critical factor determining the performance of the amplifier, and thus, the system is its bias conditions set by the power supply voltage "BiasVolt".

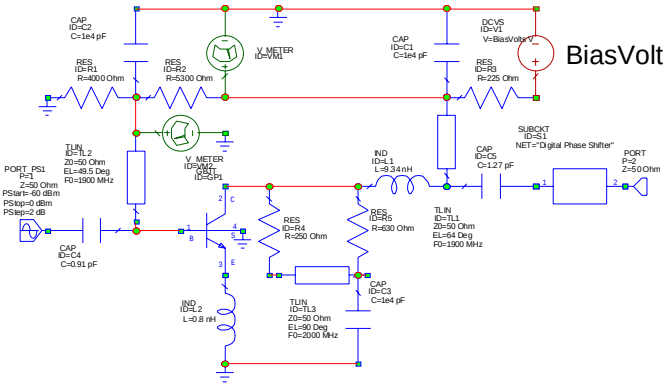

Figure 6 - 2GHz power amplifier

The objective of the simulation is to quantify the SER at the receiver as a function of a number of design parameters including the input system power, channel noise level, and, in particular, the amplifier non-linearities at different bias conditions. Shown in Figure 7 and 8 are the AM-AM and AM-PM characteristics of the power amplifier respectively. Amplitude and phase distortion will increase the uncertainty of the QAM symbols as the input power level is varied from –40dBm to –10dBm. Shown in Figure 9 is the SER associated with these different bias values. For each BiasVolt value, the amplifier circuit was simulated by harmonic balance, then non-linear behavioral models were dynamically extracted, and the system simulator was updated to determine SER. All this was accomplished by changing only a single tuning variable within the unified design environment, and the results were obtained in about a minute on a nominal Pentium based laptop. Any number of tuning variables at the circuit or system level can be defined adding to the flexibility.

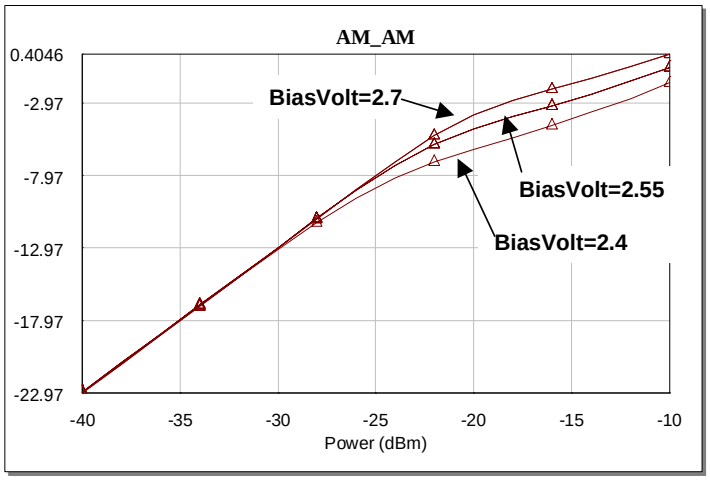

Figure 7 - Amplifier AM-AM characteristics vs BiasVolt

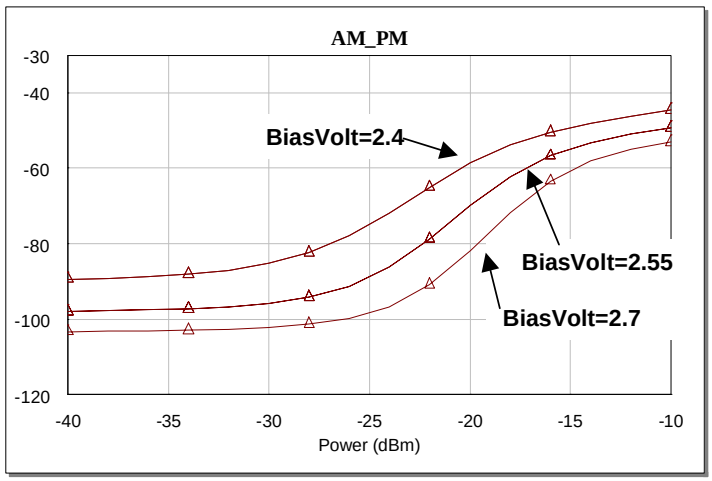

Figure 8 - Amplifier AM-AM characteristics vs BiasVolt

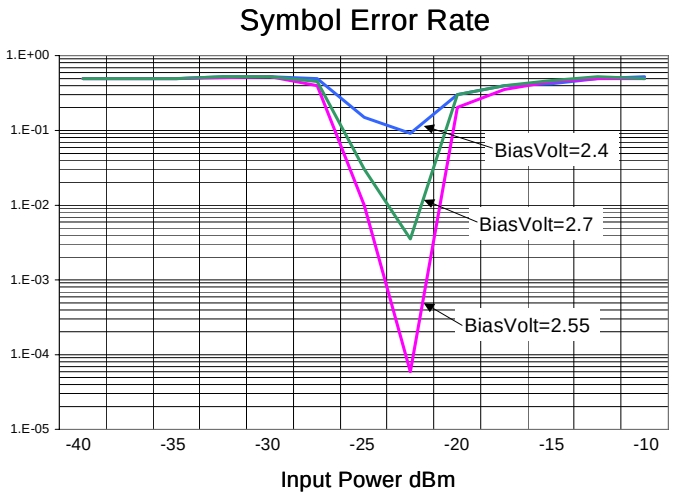

Figure 9 – SER at receiver as a function of BiasVolt

Shown in Figure 10 is a snapshot of one of the better 32 QAM constellations obtained at the receiver. The constellation is continuously updated as the symbols are modulated and received offering additional insights as to the operation of the system.

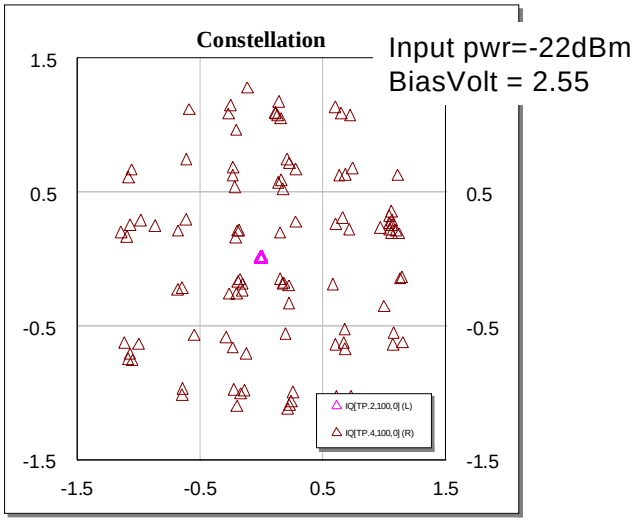

Figure 10 – QAM receiver constellation

6 Conclusion

A unified RF system and circuit design environment has been presented. With it, designers can study the impact of non-linear circuit level parameter changes and their impairments on complex communications systems specifications in real-time. This unique capability is made possible by an unmatched tool integration architecture that allows multiple simulators and analysis tools to be incrementally executed and coupled by a dynamic non-linear behavioral model generator. Real-time parameter tuning and optimization is possible at all levels of simulation offering insights never before possible. Because of its remarkable ability to bridge the gulf between RF system and circuit development, the design environment has the potential to revolutionize the design process. In doing so, it will dramatically reduce product spins and development schedules due to disconnects and inefficiencies that now exist between RF system and circuit designers.

References

[1] Brown, J, "System Simulator Melds DSP and RF Analysis", Cover Story, *Microwaves and RF*, February 2002

[2] Y. Krikorian and J. Goldstein, "A Methodology for Combining System Level and Circuit Level Simulators to Examine Trade-Offs, Constraints, and Second-Order Effects for Wireless Designs", *Elanix Application Note – AN130*, March 2 2000. - www.elanix.com/pdf/an130a.pdf

[3] Kundert, K, "Simulation Methods for RF Integrated Circuits", *Proceedings of the ICCAD 1997*