A New Methodology for Analog/Mixed-Signal (AMS) SoC Design that Enables AMS Design Reuse and Achieves Full-Custom Performance

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Abstract

Design of the analog portion of a mixed-signal System on Chip (SoC) is a recognized bottleneck for getting SoC products to market. The primary causes of this bottleneck are the lack of qualified analog design engineers and inadequate electronic design automation (EDA) tools for the analog designer. One of the most profound effects of the lack of analog design automation is the limited reuse that occurs in analog/mixed-signal design. This paper presents a new automation-based design methodology for analog/mixed-signal SoC design. This new methodology enables design reuse while providing performance equivalent to conventional full-custom analog design methodologies. We begin by presenting the new automated design methodology for analog/mixed-signal circuits based upon Neolinear's NeoCircuit® and NeoCell® tools; we then present the results of our experience using this new methodology to design a high performance SAR ADC and compare it with traditional methods for designing full-custom analog/mixed-signal circuits. We conclude by discussing the ability of this new methodology to support analog/mixed-signal design reuse and the benefits that accrue from this capability.

	Process Feature Size *X: available (X): under design or planned*		
Base Process	0.25u	0.18u	0.14u
Analog Process	0.25u	0.25u	0.25u
Normal (Vdd=2.5V)	X	X	(X)*
Low Leakage (Vdd=2.5V)	X	X	(X)
Vdd=3.3V	(X)	X	
Vdd=5.0V	(X)		

Table 1. *Toshiba SAR ADC Process Line-Up*

1. Background

"Analog Cores" are a key component in system LSI or SoC applications. At Toshiba, highly skilled analog design engineers are needed to design core analog functions such as Phase Locked Loops (PLLs), Analog-to-Digital Converters (ADCs), etc. Using conventional design flows, the same level of design experience and effort is required to port these previously designed core analog functions, even when a similar process is used. Table 1 illustrates the process line-up for the Successive Approximation Register (SAR) ADC that is the subject of this paper.

To reduce the effort required to port analog cores from one process to another, Toshiba is implementing a new AMS design methodology that enables significant analog design reuse. A benefit of this new methodology is that valuable AMS design engineering resources previously needed for porting can be shifted to the design of new value-added analog cores.

In the following sections we detail our experience using this new analog design methodology in the development of a 0.14um 10bit 1MHz SAR ADC utilizing the process highlighted (*) in Table 1. We begin by presenting our experience using NeoCircuit to automate the circuit sizing process. We then describe the use of NeoCell in automating the generation of the layout. In section 4 we present the results from this new AMS design process and compare it with the conventional manual-based, full-custom design process. We conclude with a discussion of the new design methodology's ability to support AMS design and the benefits expected from this new capability.

2. Circuit Design

The time required to do circuit design and the quality of the results are strongly dependant on the skill of the design engineer performing the task. An experienced engineer is able to find a good solution relatively efficiently. But in the case of a junior engineer, many design/simulate/update schematic iterations are needed to obtain a design that meets the necessary performance specifications at all required operating and process corners. This process takes a significant amount of time and requires significant hardware and software

resources. NeoCircuit significantly improves this process by automating circuit sizing.

NeoCircuit automatically sizes any circuit topology (i.e. circuit schematic) to a set of specifications using commercial or proprietary simulators [1,2,3,4]. This approach differs from other approaches, which are topology specific [5]. NeoCircuit transforms an unsized circuit topology, annotated with critical device relationships, into a sized circuit optimized to meet specifications. NeoCircuit uses the designer's simulator, testbenches and device models to evaluate automatically generated circuit solutions. This approach eliminates the need for back of the envelope calculations and a "good" starting point. Sizing may start completely from scratch, without any initial device sizing information on the schematic while respecting all design constraints.

Sizing in NeoCircuit begins with annotating the schematic database with constraints, which includes defining critical device relationships (e.g. matching), identifying independent variables and providing the target design specifications (e.g., Total Harmonic Distortion [THD]). Numerous simulations, including process and operating corner simulations, can be setup to measure the target specifications of the circuit. After sizing a circuit, designers can view trade-off curves (e.g., between two goals such as power and settling time) to quickly explore and select qualified circuits for the application.

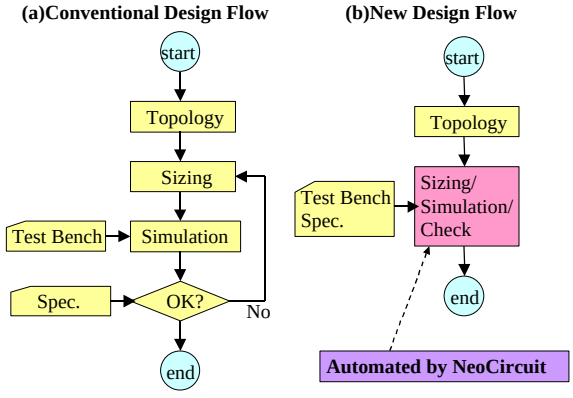

Figure 1. *Conventional vs New Circuit Design Flow*

Figure 1 illustrates the difference between the conventional design flow and the new design flow where the circuit sizing process is automated. Important benefits of using NeoCircuit include capture of the designer's knowledge about the circuit and design intent in the form of constraints. Since these constraints are technology independent, the circuit may now be easily reused – for example, automatically ported from one process to another.

All cells in the SAR ADC were automatically sized using NeoCircuit. Table 2 identifies the different cells and analyses performed. It should be noted that the automatic sizing was done not only for nominal conditions, but also for process and operating corners such as high and low Vdd, and high and low Temperature.

Cell	Analysis	Analysis Objective
Fully differential chopper comparator	AC	DC gain, ft, phase margin, Idd, CMF (Auto-zero/Amp)
	Transient	Auto-zero, gain
Resistor ladder DAC	DC	DC Accuracy, Idd
	Transient	Settling Time
Constant Current Source	DC	Iout, Idd
	Transient	Start-up time
Level shifter (Digital)	Transient	Delay, Idd
Gate delay (Digital)	Transient	Delay, Idd

Table 2. *Automatically Sized SAR ADC Cells*

Figure 2 presents an example of the NeoCircuit tool. After starting the sizing process, NeoCircuit continually updates the user interface with information about the current best circuit solution while searching the design space for other, better design solutions. This information includes the current values for each goal (design specification) and independent design variable. The user can stop the sizing run at any time, back-annotate the device sizes onto the schematic, and then restart the process. Because NeoCircuit uses the designer's simulator, testbenches and models, the results presented by NeoCircuit exactly match the results the designer obtains after back-annotation onto the schematic. NeoCircuit saves all of the design solutions that were explored during the sizing run, including candidate solutions that do not satisfy all the goals. As a result, the designer can mine the data and view design trade-off curves.

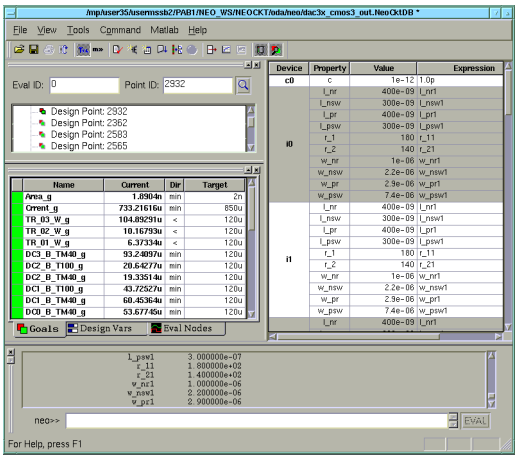

Figure 2. *NeoCircuit Example*

Table 3 compares the conventional circuit design process with the new methodology. By capturing the designer's intent in a technology independent form, the new methodology enables easy design reuse.

	Conventional (Manual Sizing)	**New (Automatic Sizing)**
Design Effort	High (depends on engineer's skill)	Low (mainly computer cycles)
Quality	Usually not optimized (depends on engineer's skill)	Optimized
Docs	Block spec/results are usually unclear	Unambiguous specs, designer's intent captured, HTML-based documentation automatically generated
Reuse (e.g., Porting)	Same effort is needed for redesign as original design	Minimal effort (e.g., point to new device models)

Table 3. *Comparison of Conventional versus New Circuit Design Flow*

3. Layout Design

Analog design requires significant know-how such as determining which devices must match, signal isolation strategies and so forth. Even if the circuit design is excellent, the layout design can destroy the circuit performance if it is not implemented correctly. Therefore the critical issue for the analog layout designer is to ensure circuit performance is not compromised by the layout. As a result, significant experience is required to do analog layout. Table 4 compares the conventional analog layout design process with the new methodology.

	Conventional (Manual Layout)	**New (Auto Layout)**
Design Effort	High (depends on engineer's skill)	Low
Quality	Good	OK (manual modification may be needed for equivalent quality)
Docs	Layout requirements are usually unclear	Unambiguous specs, layout engineer's intent captured as constraints
Reuse (e.g., Porting)	Same effort is needed for redesign as original design	Minimal effort (reuse constraints and device positions)

Table 4. *Comparison of Conventional versus Analog P&R Based Circuit Design Flow*

We have introduced NeoCell [6,7,8] as an automatic place & route tool to break through the productivity bottleneck for analog layout. Figure 3 presents an example of the NeoCell analog P&R tool.

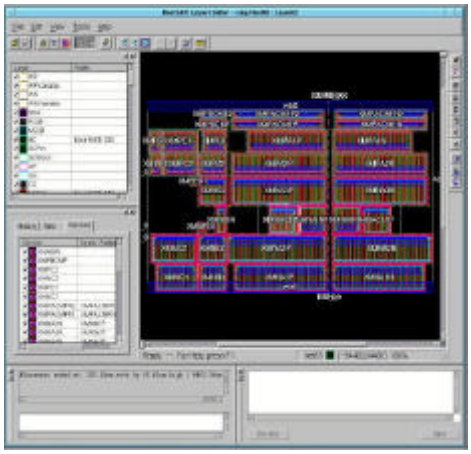

Figure 3. *NeoCell Example (Comparator)*

Traditionally, manual analog cell layout starts with a sized circuit schematic and proceeds one polygon at a time. The careful optimizations needed to handle the tight coupling between circuit and layout are managed only informally. This often means iterating over layout changes, repeatedly tweaking the geometry until no

critical analog constraints are violated. A small cell may require days for layout. A larger cell may take weeks. Worse, vital electrical and geometric constraints specified during this tedious exercise are usually lost. NeoCell fundamentally changes this tedious process. Its unique constraint-driven model captures these vital constraints and enforces them rigorously across all phases of layout. The result is that critical design information is unambiguously captured, enabling the design to be easily reused. For example, a layout may be automatically generated to meet different layout requirements (e.g., a change in required aspect ratio) or ported to a new manufacturing process. Table 4 compares the conventional analog layout design process with the new analog layout design process.

In the next section we present our results using the new design methodology, and compare these results to those obtained using the conventional design process.

4. Results

Table 5 compares the design effort required in the conventional design process with the new design methodology for the SAR ADC designed in Toshiba's .14um, 2.5v manufacturing process currently in development (see Table 1). Design effort is presented in designer-weeks (w) and designer-days (d). As shown in Table 5, significant improvements in circuit and layout design productivity were realized using the new design methodology compared with the conventional methodology. With regards to the resistor DAC, the new methodology required as much time as the old methodology but produced significantly better results (see comments).

The most interesting comparison in Table 5 is the difference in circuit design time required for the Chopper Comparator. Using the old design process, four designer-weeks were required for circuit sizing compared to one designer-day using the new methodology. This bottleneck is due to the difficult nature of the design task where minimal headroom, resulting from the seven-transistor stack and the 2.5v process, introduced many design variables that had to be simultaneously considered by the designer. Significantly, the designer's intent is now captured as an immutable part of the design database, enabling easy reuse.

Table 6 presents critical parameters for the SAR ADC. Since the new design is required to operate 7x faster than the original design (10 bit 7us versus 10 bit 1us), a direct comparison is difficult. However, an analysis by Toshiba's designers indicates the new process provides results equivalent to or better than conventional, full-custom manual design.

	Old Design	New Design	Ratio
Base Process	0.18um	0.14um	-
Analog Process	0.25um	0.25um	-
Spec	10bit 7us ADC	10bit 1us ADC	0.14
Idd	0.4mA	0.5mA	1.25
Iref	0.22mA	0.75mA	3.41
Core Size	0.52mm x 0.34mm	0.45mm x 0.41mm	1.04

Table 6. *Design Performance – Conventional versus New Design Methodology*

Cells	Circuit Design		Layout Design		Comments
	Old	New	Old	New	
Chopper Comparator	4w	1d	3w	3d	✓ Difficult design ✓ 7 transistors stacked in 2.5v process
Resistor Ladder DAC	1w	1w	3w	n.a.	✓ Previous design did not meet settling time specification ✓ New design is more difficult (settling time requirement 7x faster)
Constant Current Bias	3d	1d	2w	.5d	✓ Previous design not optimized for operating/process corners (e.g., Vdd, Temp)
Gate Delay	2d	0.5d	1d	n.a.	✓ Digital Circuit
Level Shifter	2d	0.5d	1d	n.a.	✓ Digital Circuit

Table 5. *Design Effort – Conventional versus New AMS Design Methodology for SAR ADC*

Figure 4 presents the final SAR ADC layout generated using the new methodology.

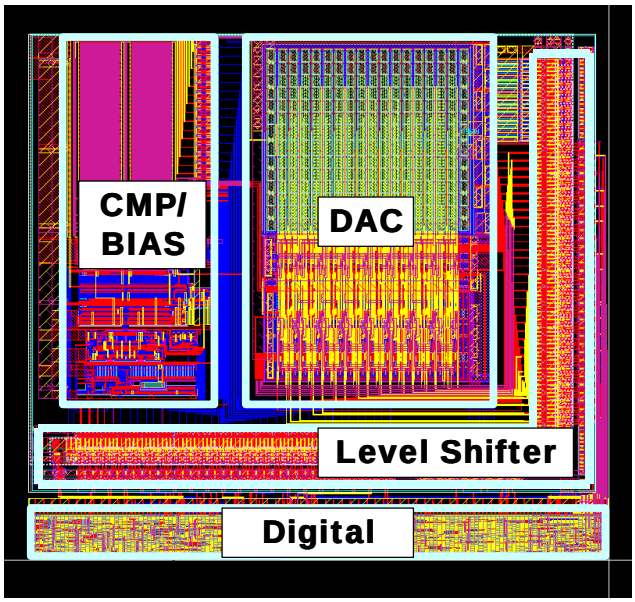

Figure 4. *SAR ADC Layout (0.45mm x 0.41 mm)*

5. Conclusion

Figure 5 summarizes manpower effort for the conventional design process, the new design methodology, and expected future benefits from the new design methodology due to increased reuse. Results from the SAR ADC design, and preliminary porting results indicate at least a 2x reduction in manpower using the new design methodology.

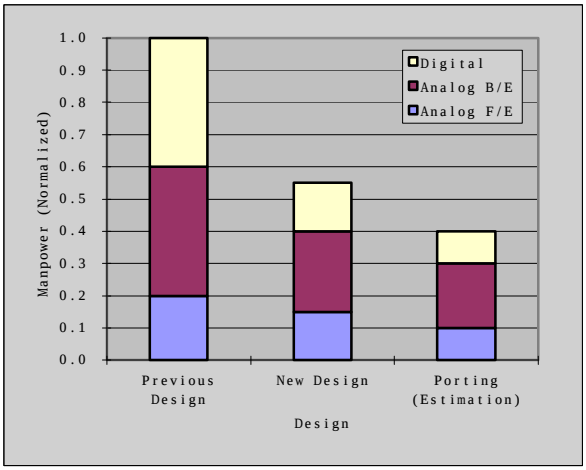

Figure 5. *Manpower Comparison*[1]

[1] Previous: First trial for digital synthesis flow. New: First trial of new AMS design flow using NeoCircuit/NeoCell in production.

Preliminary experience with the new design methodology indicates that an expert engineer best performs the initial design since significant know-how is valuable in capturing this design knowledge as reusable design constraints. Once the expert knowledge is captured in a reusable form, less-experienced engineers can easily perform design tasks such as porting because they can re-use the design knowledge (constraints).

By using NeoCircuit/NeoCell to develop a new, automated analog design flow, both the analog and digital blocks are becoming synthesizable, as shown Figure 6.

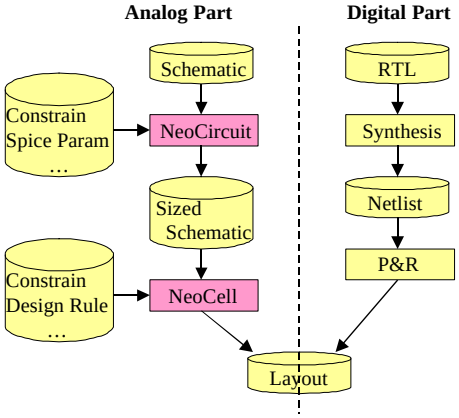

Figure 6. *Automated AMS Design Flow*

Not unexpectedly, the automated analog design flow is not as advanced the digital design flow. The flow would benefit from additional capabilities. For example:

- Automatic topology selection
- Block-level circuit synthesis
- Automatic generation of behavioral AMS models
- Feed-forward of circuit information to layout, such as identification of parasitically sensitive nodes, net sizing to meet electromigration rules based upon simulated current, etc.
- Automated AMS floor-planning and hierarchical analog layout
- Signal path recognition and knowledge of current flow
- Fully automatic analog layout

However, even though the automated analog flow is new compared to the conventional manual full-custom analog design flow, there are already major improvements in three important areas:

- Reduced design time for initial design compared to the conventional manual flow
- Equal or better design quality
- Reuse of analog/mixed-signal designs is now possible, resulting in the ability to leverage experienced designer's knowledge to achieve dramatic improvements in productivity

With the new design flow, development of real analog IP is now possible.

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