A New Methodology for AMS SoC Design that Enables AMS Design Reuse and Achieves Full-Custom Performance

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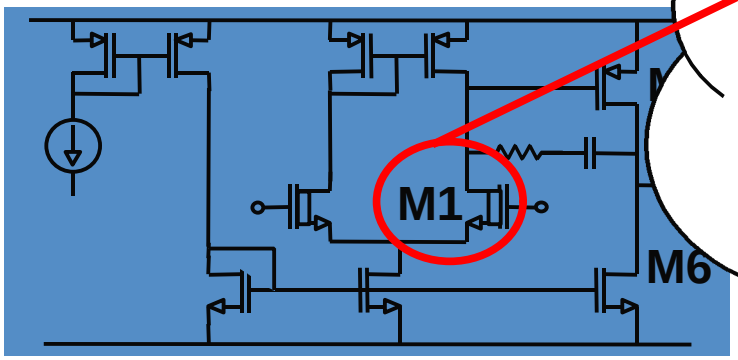
Overview

- Background
- Circuit Design
- Layout Design
- Results
- Conclusion

Analog Circuit Sizing: Manual Process



How do I determine M1's W?

Does W1 affect my second pole?

gain = -gm1*(gds5||gds6)

How can I minimize power? Area?

How does W1 affect noise?

$I_D = (u_n C_{ox}/2)(W1/L1)(V_{GS}-V_{tn})^2$

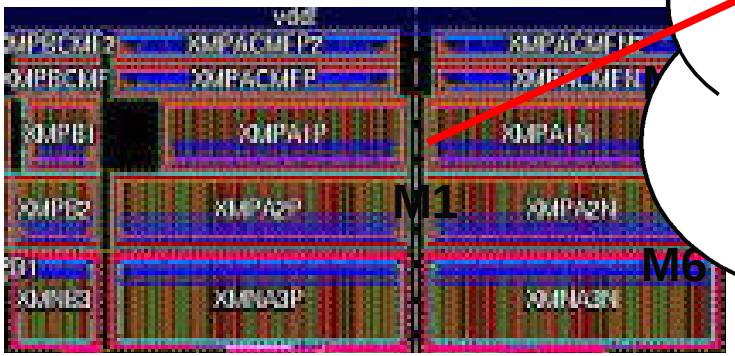
What specs does W1 affect?

Is this even the right topology?

#*$&, this is hard!

- Must solve assumption-based equations
- Manual tuning almost always required
- Manually balance tradeoffs
- Limited re-use

Analog Layout: Manual Process



How can I be sure my devices match?

spacing, orientation, interdigitation

How do I route to all of my requirements?

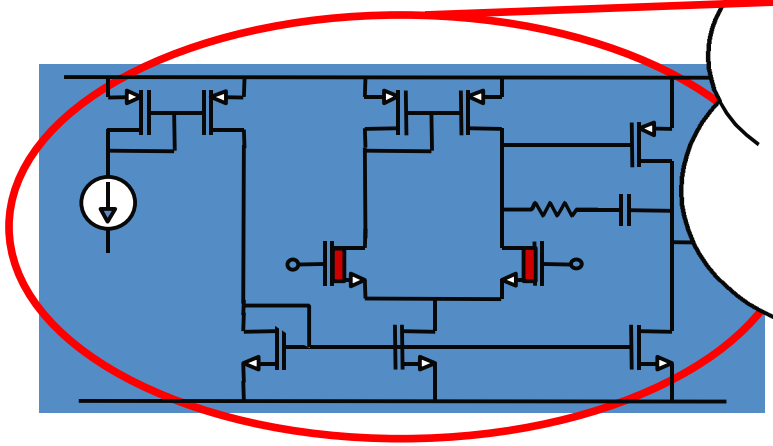
crosstalk, balancing, electromigration

How can I be sure my intent was communicated properly?

#*$&, am I frustrated!

- Analog layout requires skilled engineer
- Manual verification of requirements
- Manually balance tradeoffs

Sizing and Layout with New Process

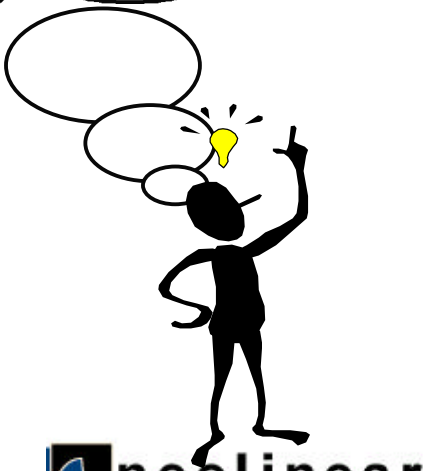


I can let NeoCircuit determine W1, W2, R1, C0...

NeoCell will P&R my layout according to my constraints.

NeoCircuit and NeoCell will help me make the right tradeoffs.

This is much easier!



- New analog design process captures design intent
- These annotations/constraints simplify technology migration and retargeting
- Circuit sizing and layout are automated

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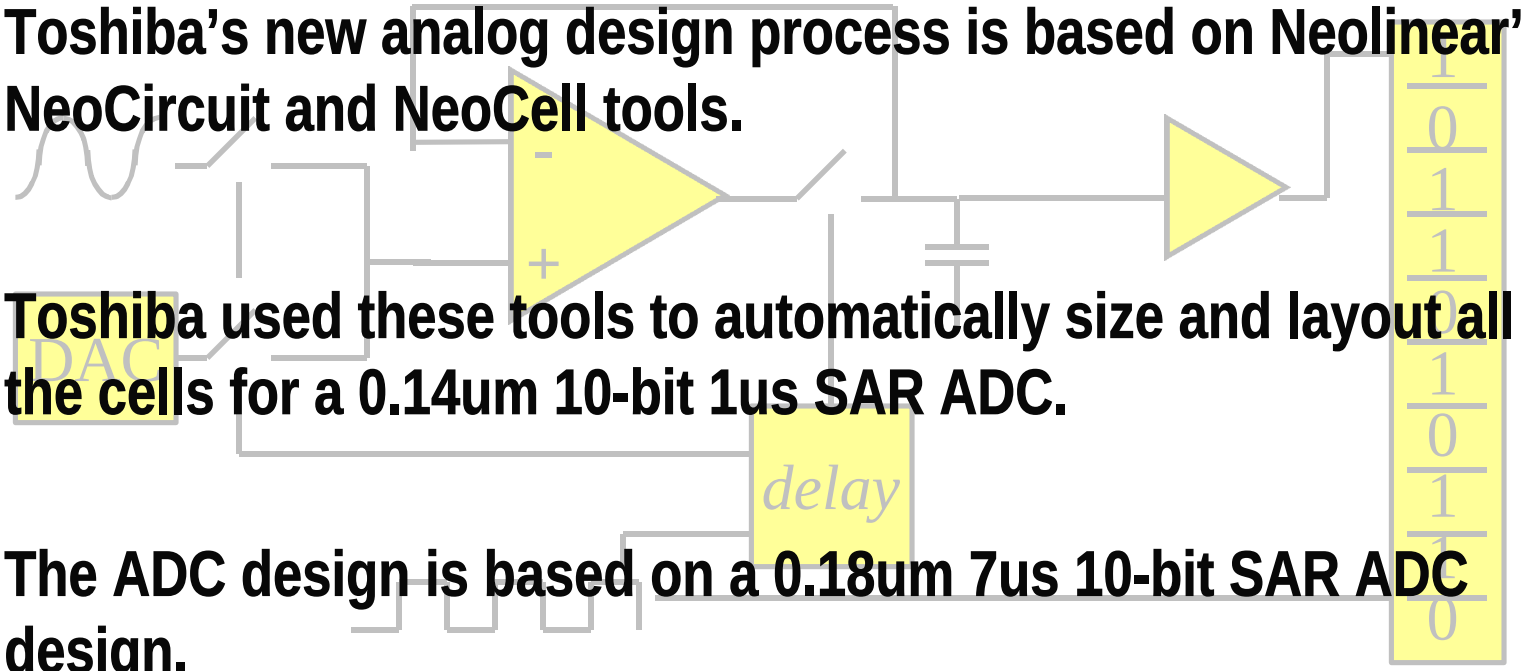
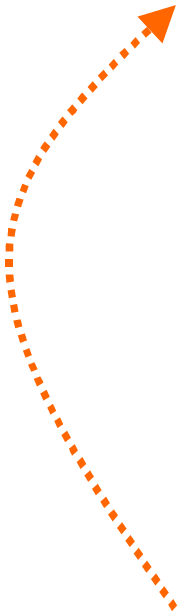
Case Study: Analog-Digital Converter

- Toshiba's new analog design process is based on Neolinear's NeoCircuit and NeoCell tools.
- Toshiba used these tools to automatically size and layout all the cells for a 0.14um 10-bit 1us SAR ADC.
- The ADC design is based on a 0.18um 7us 10-bit SAR ADC design.



Circuit Design: List of Cells

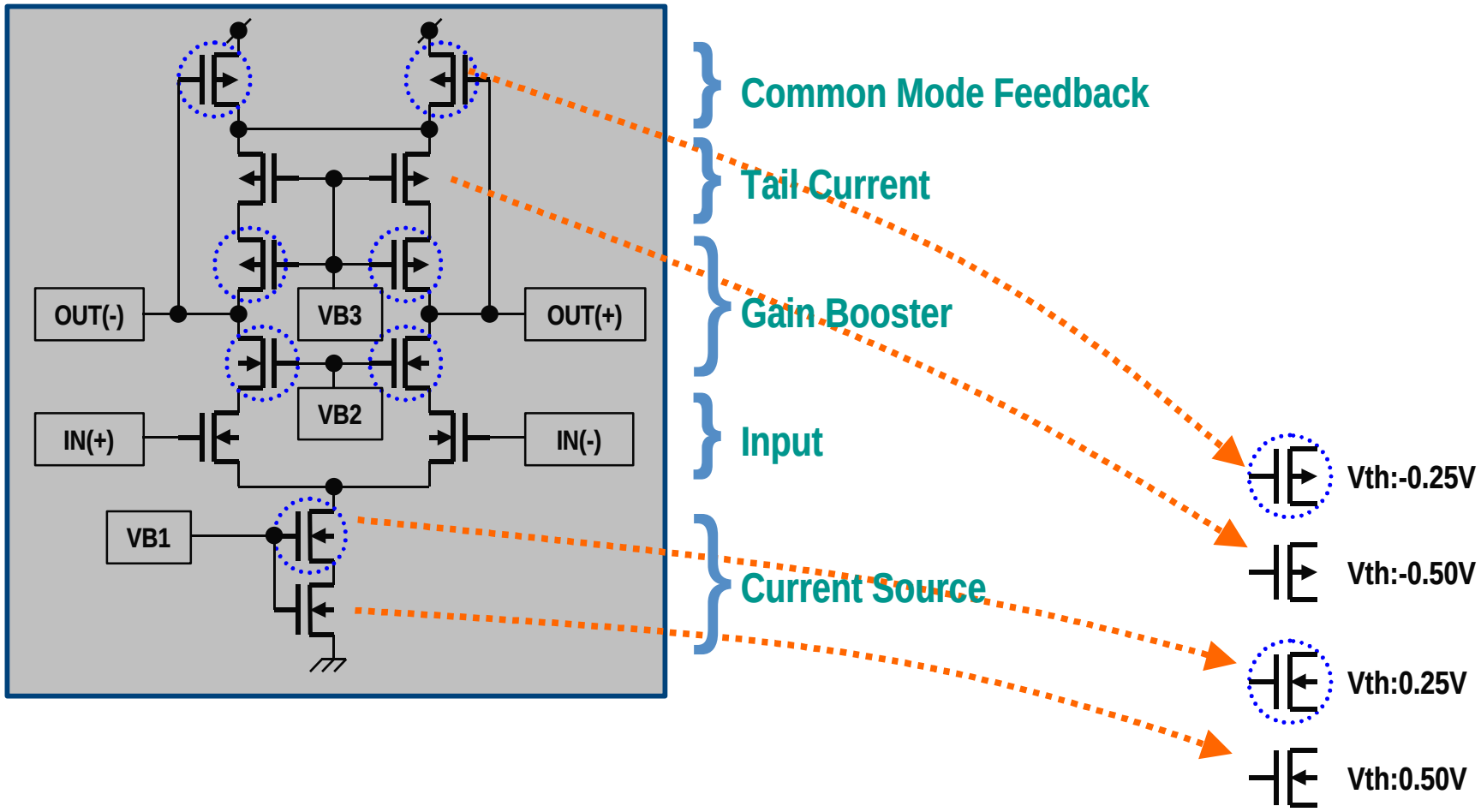
Circuit	Analysis	Specification(s)
Full-Diff Chopper Comparator	AC	DC-Gain, ft, Idd, CMFB
	Transient	Auto-zero, gain
Resistor ladder DAC	DC	DC Accuracy, Idd
	Transient	Settling time.
Constant Current Source	DC	Iout, Idd
	Transient	Start-up time.
Level Shifter	Trasient	Delay, Idd
Gate Delay	Transient	Delay, Idd



hard to design manually

Circuit Design: Comparator Circuit

7 Transistors Stacked in 2.5V Process!



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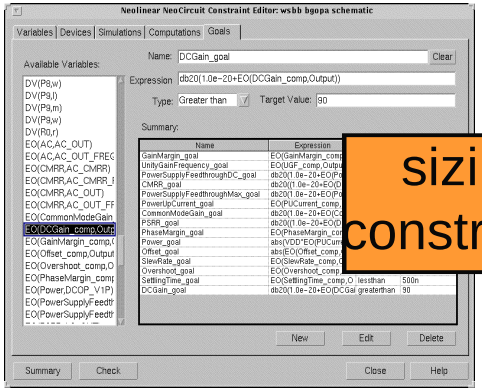
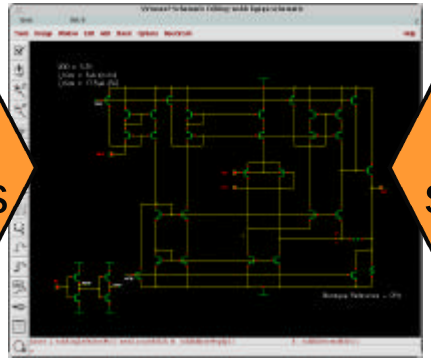
Analog Circuit Sizing with NeoCircuit

Cadence DFII



NeoCircuit
constraint editor

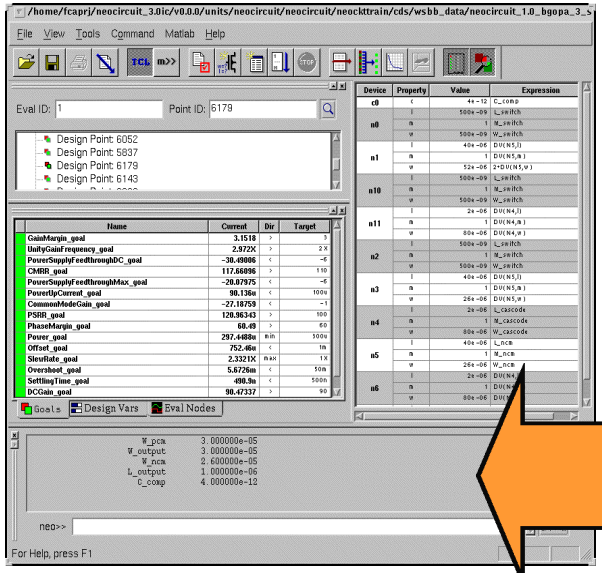
sizing
constraints



unsized
schematic

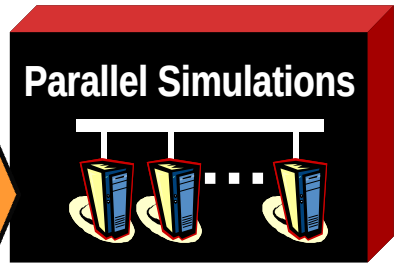
Toshiba
Topology
database

result
back annotation



NeoCircuit
sizing engine

Spectre, HSPICE



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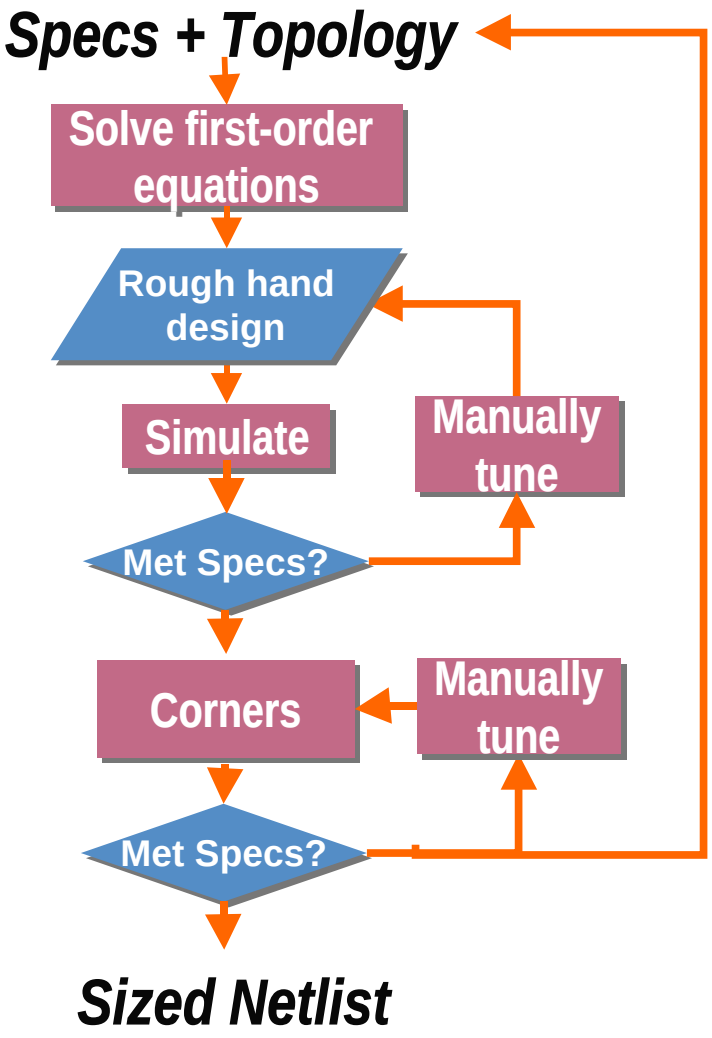
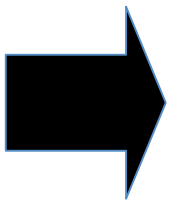
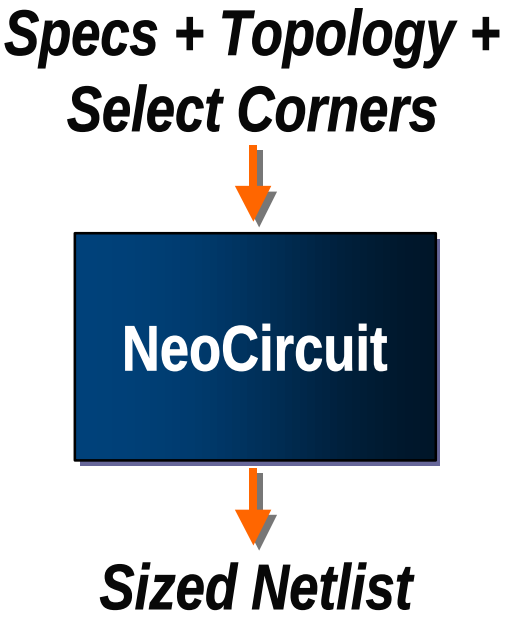
Manual Circuit Sizing vs Automated Circuit Sizing

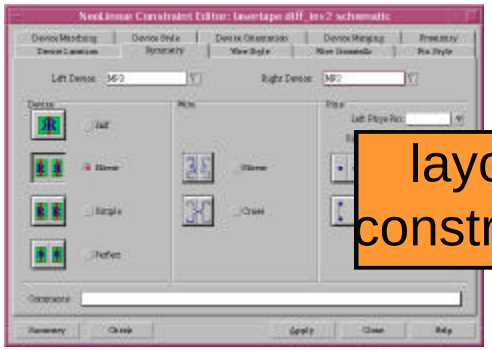




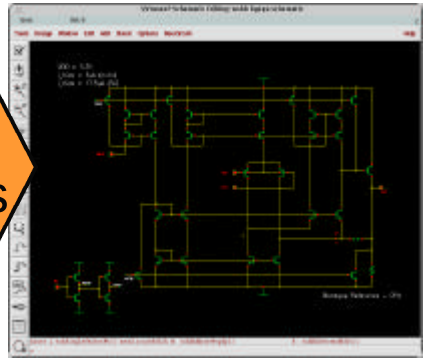


Analog Circuit Layout with NeoCell

Sized Schematic



layout constraints



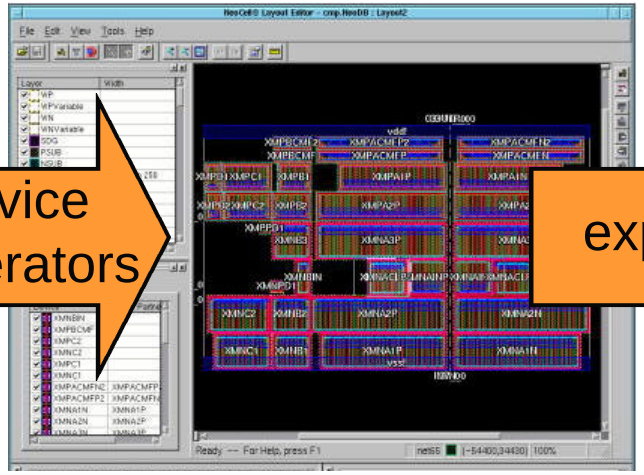
NeoCell Constraint Editor

Virtuoso

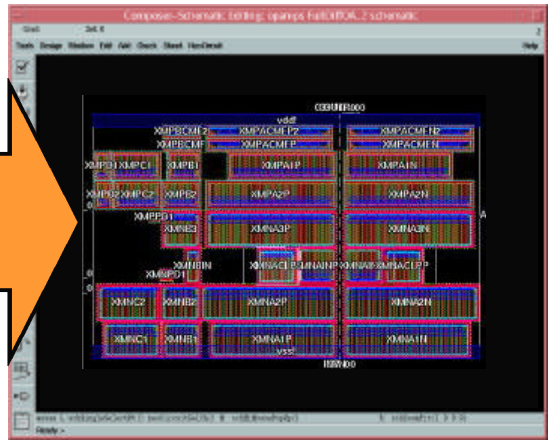
Cadence PCELL

NeoCell MODGEN

device generators



export



NeoCell APR

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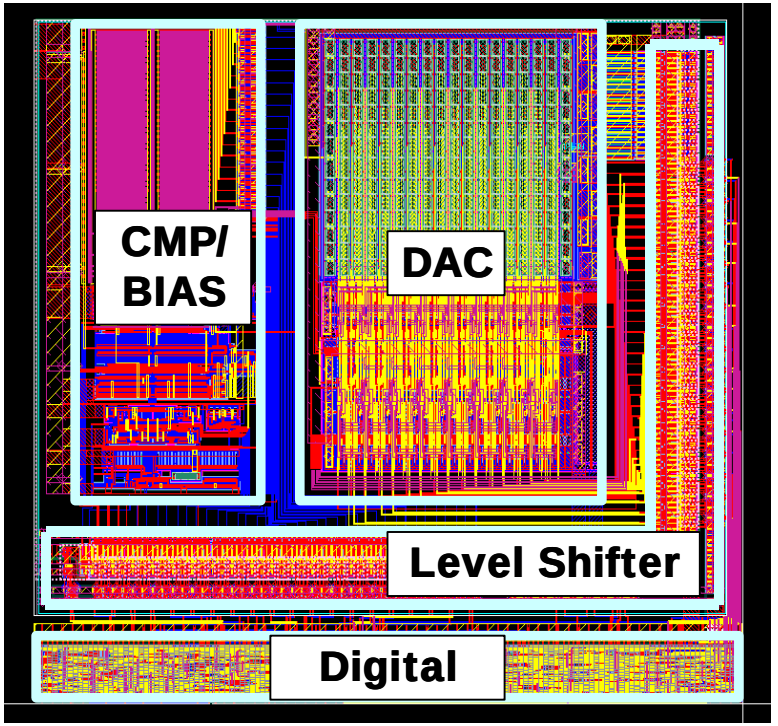
Results

	Original Design	New Design
Base Process	0.18um	0.14um
Analog Process	0.25um	0.25um
Res/Speed	10-bit/7us	10-bit/1us
Idd	0.4mA	0.5mA
Iref	0.22mA	0.75mA
Core Size	176800sqr um	184500sqr um



Results

Cell	Circuit Design		Layout Design		Comments
	Old	New	Old	New	
Chopper Comparator	4w	1d	3w	3d	✓ Difficult design ✓ 7 transistors stacked in 2.5V process
Resistor Ladder DAC	1w	1w	3w	n.a.	✓ Previous design did not meet settling time specification ✓ New design settling time requirement is 7x faster
Constant Current Bias	3d	1d	2w	0.5d	✓ Previous design not optimized for operating/process corner
Gate Delay	2d	0.5d	1d	n.a.	✓ Digital Circuit
Level Shifter	2d	0.5d	1d	n.a.	Digital Circuit

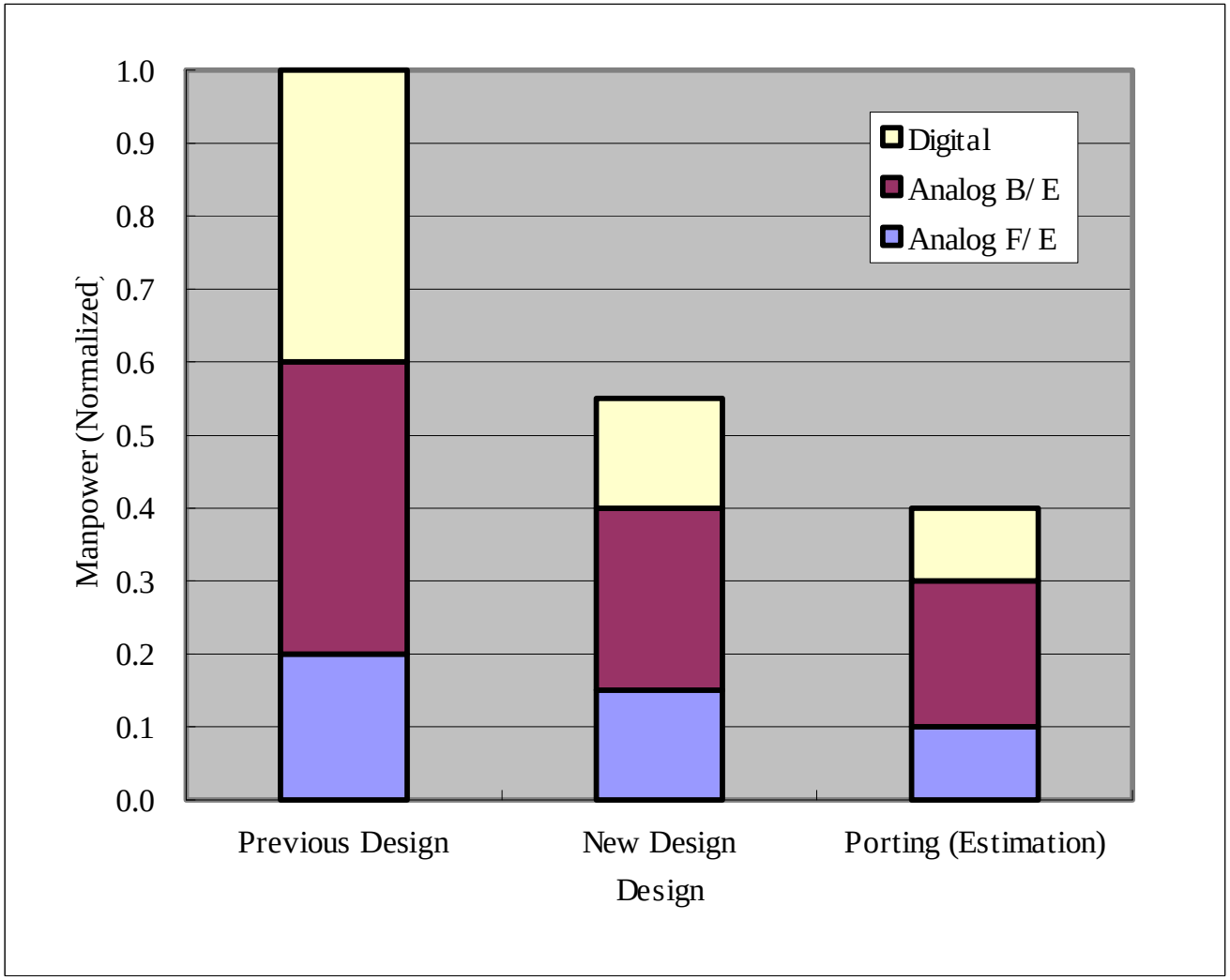
Conclusion: Circuit Design

	Conventional (Manual Sizing)	New (Automatic Sizing)
Design Effort	High (depends on engineer's skill)	Low (mainly computer cycles)
Quality	Usually not optimized (depends on engineer's skill)	Optimized
Docs	Block specs/results are usually unclear	Unambiguous specs, designer's intent captured, HTML-based documentation automatically generated
Reuse (e.g., Porting)	Same effort is needed for redesign as original design	Minimal effort (e.g., point to new device models)

Conclusion: Layout Design

	Conventional (Manual Layout)	New (Analog P&R)
Design Effort	High (depends on engineer's skill)	Low
Layout Quality	Good	OK (manual modification may be needed for equivalent quality)
Docs	Layout requirements are usually unclear	Unambiguous specs, layout engineer's intent captured as constraints
Reuse (e.g., Porting)	Same effort is needed for redesign as original design	Minimal effort (reuse constraints and device positions)

Conclusion: Design Effort



Summary

- Reduced design time for initial design
- Equal or better design quality
- Designer intent is fully captured
- Reuse of analog/mixed-signal designs is now possible