Agenda

- Traditional signoff points
- Determination of signoff points
- Conclusion

Traditional Sign-off Points

- *What is a signoff point?*

  The point at which the silicon provider accepts a design. From that point, the customer expects significantly less involvement, and working prototypes yesterday.

Traditional Sign-off Points

- *GDSII*
- *Netlist*
- *Placement*
- *RTL*
- *Specification*

Traditional Sign-off Points

- GDSII
  - In use for over 20 years
  - Customer assumes significant liability
  - Technology complexity (signal integrity) means fewer customers will be able to handle this engagement model
  - Design complexity (M's of gates, >100 memories, Hi-performance system, Hi-speed I/O, complex packaging, thermal issues, multiple on-chip processors) means fewer customers can handle this engagement model
  - Up to .11um, this was a more viable sign-off point than it is now

Traditional Sign-off Points

- Netlist
  - In use for over 20 years
  - Majority of designs today
  - No longer "golden netlist" with physical resynthesis, test, buffering & signal integrity modifications
    - Recognizable with original netlist only through formal verification
  - Both RTL coding & synthesis mistakes have accumulated up to this point
    - Congestion & Timing problems start with RTL & are made worse through synthesis

Traditional Sign-off Points

- Placement
  - Reduces problem of delivering incomplete constraints, poor quality netlist, inaccurate wireload models
  - Avoids iterations between customer & silicon provider
  - Becoming too approximate a signoff point to be final placement, while mostly ignoring: power, clock, I/O critical logic, package, xtalk, test, global route, congestion analysis
    - Next generation synthesis might be needed
  - This model is likely to remain "seed placement" signoff as it is today

Traditional Sign-off Points

- RTL
  - Functionally correct & physically incorrect most of time
    - More than 30 designs evaluated
  - Many designs are signed off at this point, with a more variable cost engagement model
  - Typically customer resource constraint & expertise driven
  - This engagement model has been influenced the most by more recent EDA developments
    - Key is the ability to evaluate timing, constraints, and area

Traditional Sign-off Points

- Specification
  - Provides the most room for optimization
  - Can partition into multiple designs
  - RTL coding for both testbench & silicon followed by gate-level synthesis
  - A few designs are signed off at this point, with only a variable cost engagement model
  - Specification must be very clear or engagement quickly becomes cost prohibitive

Determination of Sign-off Points

- Whoever is responsible for the silicon working should own the signoff model
  - This flexible & variable model should be jointly agreed upon by whoever owns silicon responsibility & whoever is paying for the first silicon development
- It's not about what tools are used; it's about matching customer expertise & bandwidth with silicon supplier expertise & bandwidth

Conclusion

- *Many sign-off models exist & will continue to exist*
- *Netlist & RTL sign-off will remain the most common signoff points due to technology and design complexity at .11um and below*
- *Tool development will influence, but not determine, sign-off models*
- *Sign-off is dependent on the customer engagement model -- the right model for the right customer*