Noise in RTL Flow

Vivek Joshi
Intel Corp.

Motivation

- Noise failures hard to debug.
- Hard to isolate. Failures are seemingly random.
- Conventional methods fail, impossible to run tests to determine failure.
- Expensive, imagine a failure on a certain bit pattern, how do you reproduce it in lab?

Introduction

- Current RTL Flow Closure Steps
  - Timing
  - Formal Verification
- Noise important and getting more important.
- Relatively new, but critical to chip success.
  - Noise failures hard to debug and happen after chip manufactured.

Noise

- RTLers need to be more aware of noise.
- Cannot use certain constructs such as tristate busses.
  - Tristate busses do not allow for repeaters.
- Timing changes due to repeaters, need to plan ahead.

Sources of Noise

- IR-drop
  - Power grid, needs to be designed well.
  - Supply charge quickly to avoid voltage droop.
  - Drain away charge quickly to avoid ground bounce.
- Inductive Noise
  - Leads used to supply power to chip.
- Capacitive Coupling
  - Transitioning signal, impacts neighbors.

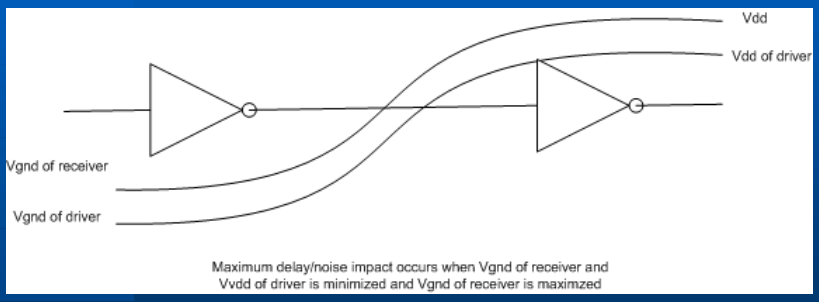
Voltage Droop

- Reduces Power available for xtors.
  - Decreases noise margin for gates.
- Inductive Effects
  - Frequency increases, this gets worse
- Interconnect Resistance
  - As interconnect layers increase, gets worse, copper helps, but …
- Ameliorated by decoupling cap in big drivers

Ground Bounce

- Same issues as Voltage Droop
- No clean solution, cannot decrease wire resistance (process controlled)
- Good power grid is the only solution.
- Design and place big drivers away from each other. RTLer needs to be layout aware.

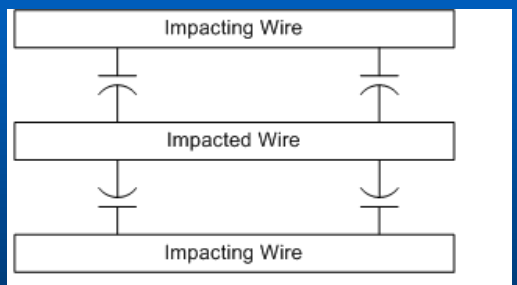
Power Grid Design Issues



Capacitive Coupling

- Chip frequency increases, coupling get worse.
- Normal solution is to decrease cross-coupling cap as % of total cap.
  - Use buffers (not always possible due to timing).
  - Slow down impacting signal. (can cause speed path)
  - No help for tristates.

Capacitive Coupling (contd.)



Cross capacitance impact:
Dependent upon attacker slope.
Can reduce slope, but then cross bar current increases, leading to higher power dissipation
Normal fix is to place buffers, but not always feasible, timing/congestion impact
Buffers hard to place for tristate signals.

Conclusion

- Noise big issue for ASICs going forward.
- Noise needs to be incorporated in tapeout flow.
- RTLer needs to be noise aware.
  - Coding guidelines from tools.
  - Block placement at full-chip level.
    - Timing and area impact of buffer addition.
  - Multiple input switching can cause min-delay's, i.e. functional failures.

Conclusion (contd.)

- Correct by construction libraries.
  - Decoupling cap inserted for big drivers.
    - Save packaging cost, but can increase leakage power.
- Power grid needs to be carefully designed.
  - Proper design, (reduces IR drop) makes more power available for xtors, might be able to get few extra MHz..