Providing Physical Vision to RTL Designers

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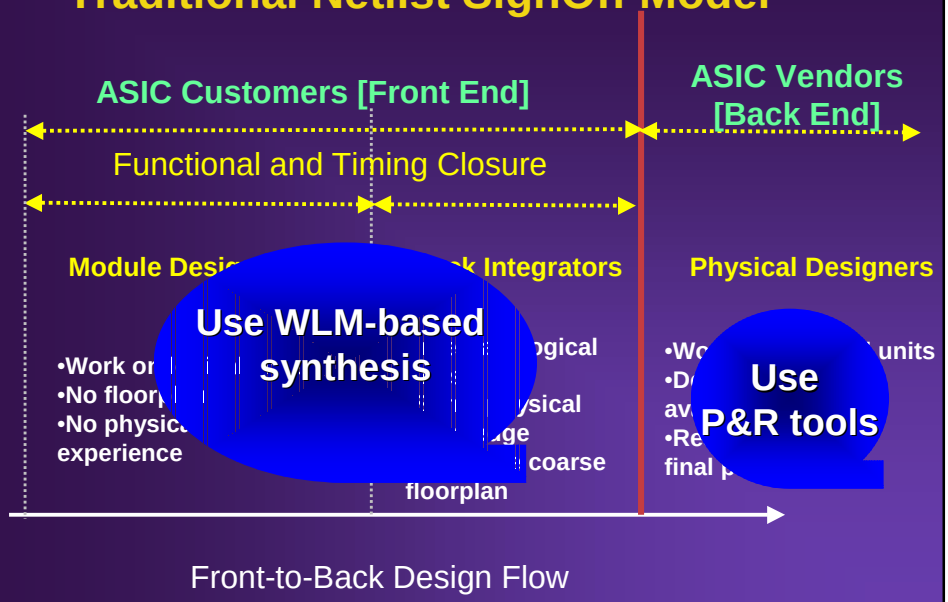
1

Traditional Netlist SignOff Model



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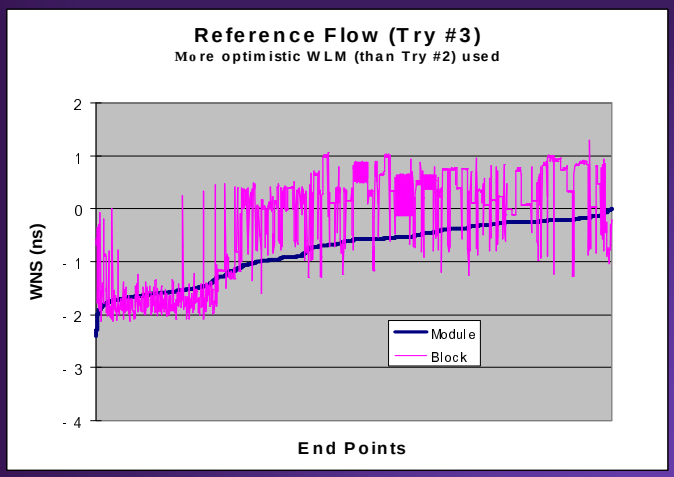
Timing Critical Designs: Performance Prediction is a Challenge



3

SignOff Models are evolving

- **Problems with traditional netlist SignOff model for timing-critical designs**
  - Longer time to convergence
  - Missed performance targets
- **As a result, new SignOff models have emerged**
  - RTL SignOff
  - Placement SignOff

4

New SignOff Models

- **RTL SignOff**
  - RTL and constraints are handed off
  - ASIC vendor responsible for synthesis, P&R
  - ASIC customer responsible for RTL development/verification and design constraint specification
- **Placement SignOff**
  - Netlist, placement, floorplan and constraints are handed off
  - High-level of predictability in performance
  - Requires P&R specialist in front-end team to drive floorplanning process

5

RTL SignOff Model

- **ASIC vendors can achieve certain level of performance**
  - By using physical synthesis tools
  - But no flexibility to change RTL
    - This is an expensive and time consuming process
- **Design constraint specification is an iterative process**
  - Needs knowledge about the design (which ASIC customers know best)
  - Needs accurate timing analysis that factors layout implications (which ASIC vendors know best)
- **Model is not scalable as implementation effort will shift to the vendor**

For timing-critical designs, intensive communication between ASIC customer and ASIC vendor

6

Placement SignOff Model

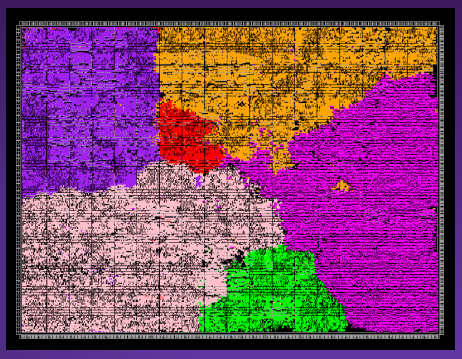
- **This model offers greater predictability compared to RTL/Netlist SignOff models**
- **Offers ASIC customers "layout-sensitive" timing estimates resulting in:**
  - RTL that is feasible for physical implementation
  - Design constraints that are realizable
- **However, this must not require ASIC customers to become layout experts**

Solution: Physical Prototype generation during RTL synthesis

7

Intuition for Physical Prototyping during RTL synthesis

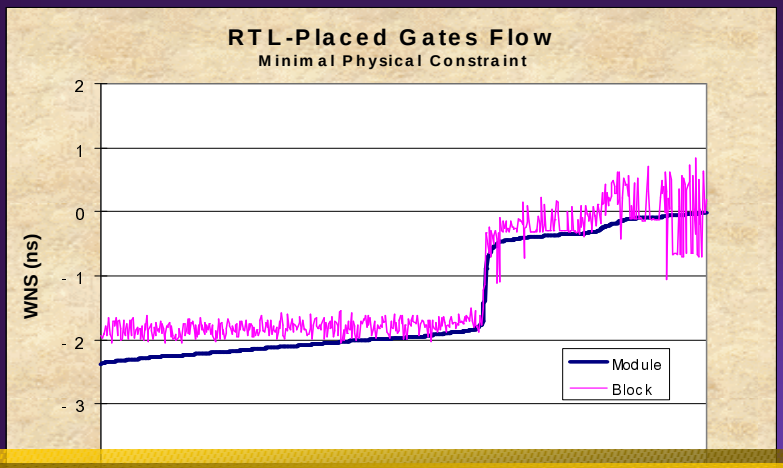
- **Spatial locality maintained for modules/blocks during placement**
- **Leverage this behavior to auto-generate physical prototypes for modules/blocks**
- **Provide flow with very low cost of adoption for a RTL module designer**
  - Has little or no knowledge of physical design



Design Placement Colored by Logical Hierarchy

8

Performance Prediction with Physical Prototyping during RTL Synthesis



Allows designers to identify real critical nets during module compiles

9

Summary

- RTL SignOff and Placement SignOff have been proposed as alternatives to traditional netlist SignOff model
- RTL SignOff limits performance goals that can be achieved due to its restrictions
- Placement SignOff improves predictability but needs to reduce the cost of adoption for front-end designers
- Quality of SignOffs can be improved dramatically by introduction of RTL physical prototyping technology in logic synthesis

10