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Managing Risk in Block Based Designs: A Front End Acceptance Methodology

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22-23 April 2002

Front-End Acceptance

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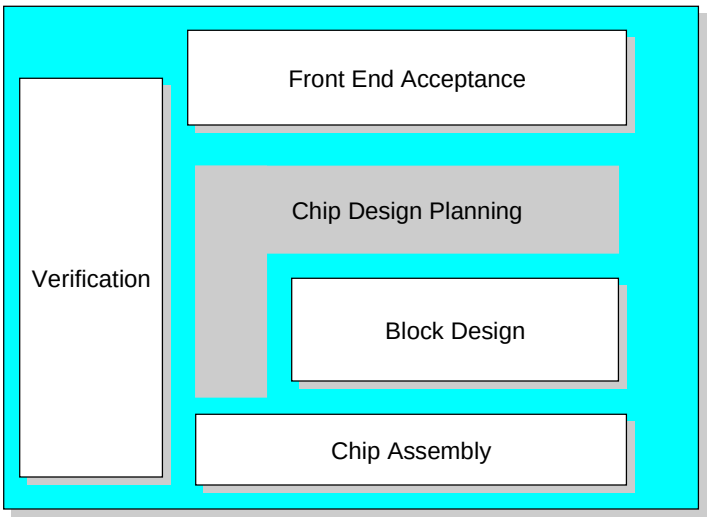
A methodology for the analysis of a proposed chip design consisting of various functional blocks that enables the design team to determine the integrity of design data, evaluate associated design risks, and develop design budgets and plans

Outline

- Block-Based Design Overview
- Front End Acceptance Flow
- Conclusion

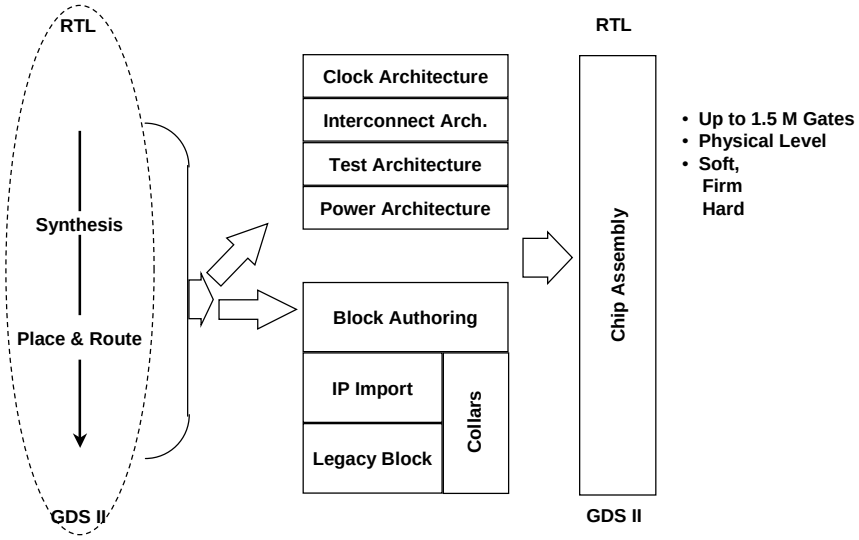
3

Block-Based Design Overview



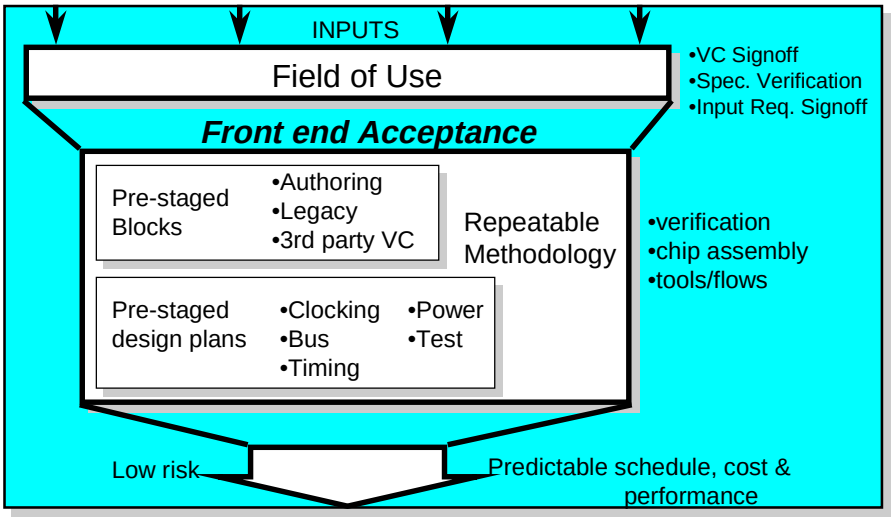
4

Block-Based Design (BBD)



5

Verification of BBD



6

Field of Use

- Digital CMOS
- .25 → .18µ technologies
- 150K → 1.5 M gates
- A/MS blocks restricted to:
  - blocks specified by VSI 1.0, A/M-S VSI Extension
  - e.g., PLLs, A/D, D/A, and hard blocks
- Import cores, mc, and mp as hard or firm;
- Technology rules, cell libraries, hard blocks, memory generators and data path blocks are fully defined and qualified
- Synchronous (~ 80 MHz)
  - multiple clock domains: All domains are integral multiples of the lowest freq. domain
- Multiple levels of hierarchy
  - deal with only two at one time
- Embedded bus architecture
  - not pre-designed
  - no previous layout (I.e custom)
- single or mixed voltages for A/MS blocks only
- Blocks created using enhanced TDD process for both VHDL and Verilog

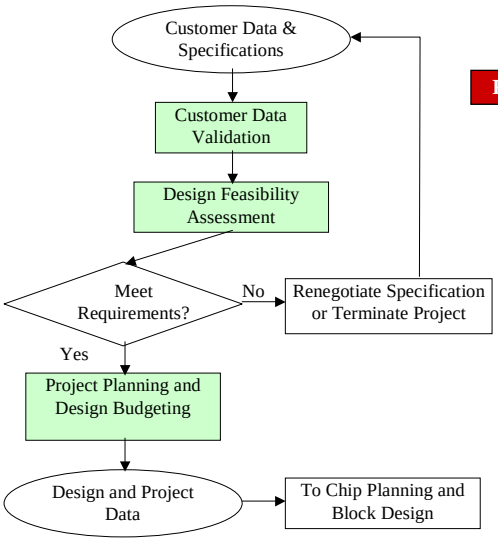
7

Front End Acceptance Purposes

- Align expectations of system designers and chip design teams
- Ensure that all required data to complete the chip design has been assembled
- Develop program commitments with associated risk factors :
  - Cost
    - Engineering & Manufacturing
  - Schedule
  - Functionality
    - Performance, area, power
- Create project data management environment
  - File structures, access control, release control, version control

8

Front End Acceptance Flow



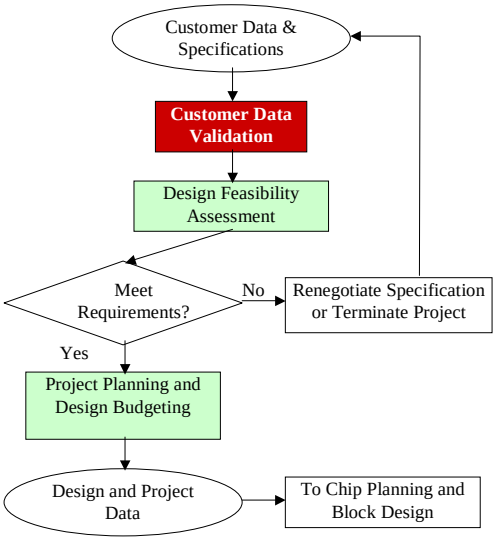
9

Field of Experience (FOE) Database

- The development and use of the BBD field of experience database involves the following processes:
  - Data gathering
    - Draws on prior designs to obtain FOE data
    - Can include projected data as well as actual data
  - Data classification
    - Groups data by application and design characteristics into an FOE database
  - Data certification
    - Verifies the data
    - Establishes the error of estimation during the FOE building and refinement stages
    - FOE data certification involves two level
      - Certification of completeness
      - Certification of accuracy
  - Data application
    - Use of the data to assess a design
    - Requires combining similar classifications to obtain statistically meaningful results

10

Front End Acceptance Flow



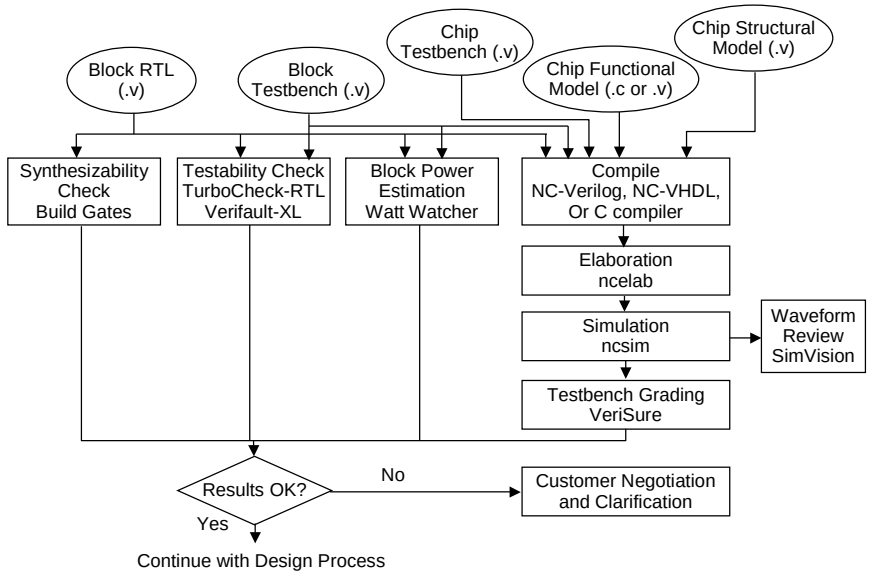
11

Customer Data Validation

- **Formal handoff of design files and requirements from system designers (customers) to chip design teams**
- **Project Checklist**
  - Documentations
  - Specifications
  - Test benches
  - Libraries
  - Models
- **Data Completeness**
  - Readability
  - Execution readiness
  - Conforms to design style
- **Simulate chip level functional model with chip testbench**
- **Simulate interconnected block functional models with chip testbench**

12

Example Tool Flow for Data Checking



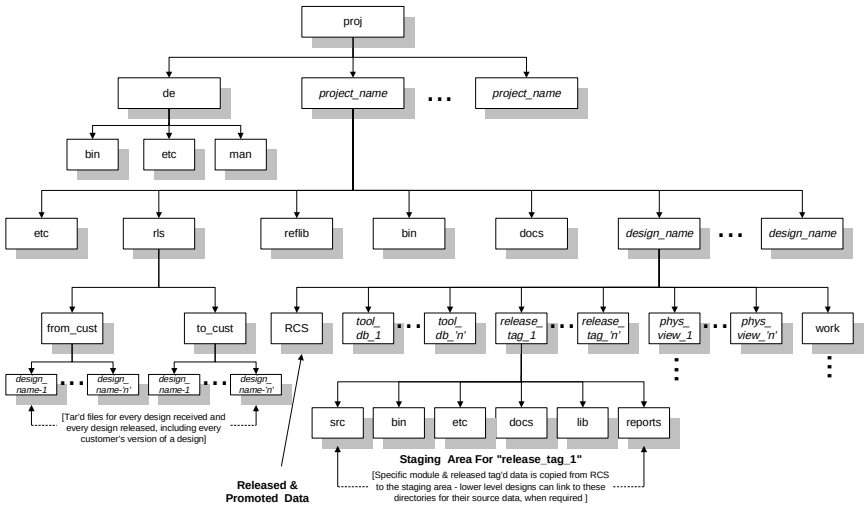
Select Preliminary Blocks

- Review block specifications against customer requirements
  - Functionality
  - Performance
  - Cost
  - Support
- Block selection matrix
  - Focus on Block characteristics within chip context
- Validate block claims & assumptions
- Can use IP Management Systems as a starting point to extract metadata about the blocks

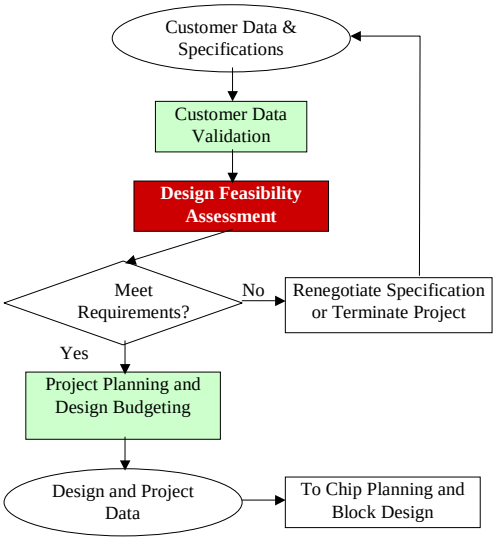
Create Project Directories

- **Hierarchical project directory**
  - Store all customer data
  - Store all design data
  - Capture all data to recreate project
    - Libraries
    - Designs
    - Utilities
    - Specifications
    - Scripts
    - Testbenches
- **Design directory hierarchy reflects design hierarchy**
- **Release control mechanism and directories**
- **Version control**
- **Access control**

Project Directory Structure



Front End Acceptance Flow



17

Design Feasibility Assessment

- Analysis of a proposed design to determine the risks in accepting the design
- Applied first at the Block level
- Then applied at the Chip level
- Three levels of refinements
  - Coarse Grain
  - Medium Grain
  - Fine Grain
- Assess key project parameters
  - Cost
  - Performance
  - Power
  - Area

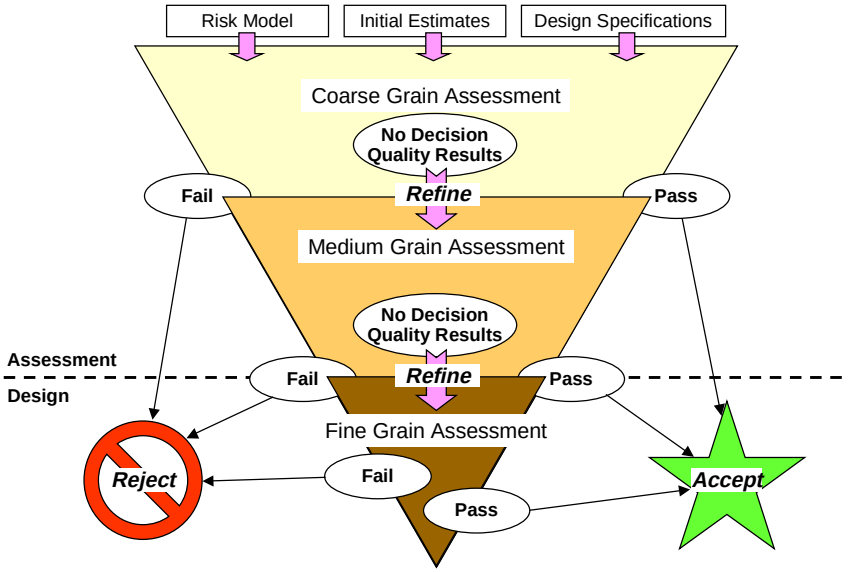
18

Design Feasibility Assessment

- **Block Level**
  - Coarse Grain Assessment
    - Based on designer experience
    - Relative to prior designs
    - ~50% error margin
  - Medium Grain Assessment
    - Based on :
      - equations
      - database
      - company field of use
    - ~20% error margin
  - Fine Grain Assessment
    - Dipping Process
    - <5% error margin
- **Chip Level**
  - Coarse Grain Assessment
    - Simple summation of block data
    - Using soft block info
  - Medium Grain Assessment
    - Weighted block assignments
    - Statistical Analysis of routing area
    - Use firm block info where available
  - Fine Grain Assessment
    - Harden critical blocks

19

Block Assessment Process



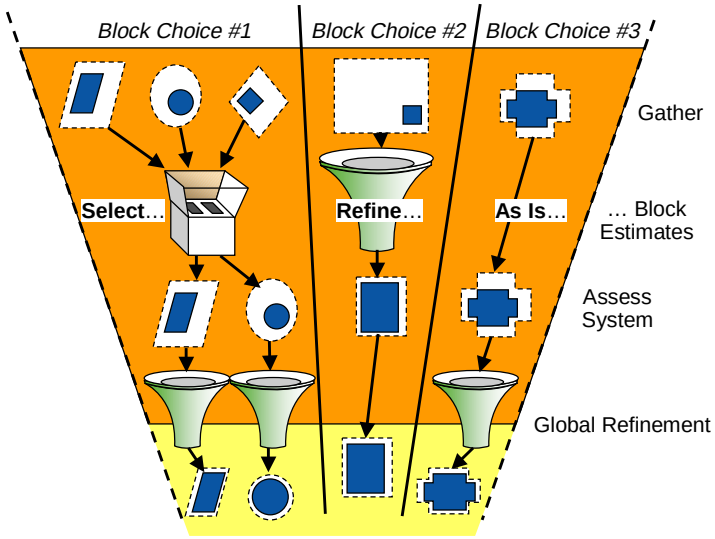
20

Chip Assessment

- Assessments performed with mixed granularity for the different elements :
  - 1st pass
    - Hard Blocks - Fine
    - Firm - Medium/Fine
    - Soft- Coarse/Medium
    - Authored - Coarse
    - Interconnect - Coarse
  - Subsequent Passes
    - Assign weighting factors to blocks based on criticality
    - Refine granularity on a block by block basis based on impact on total design

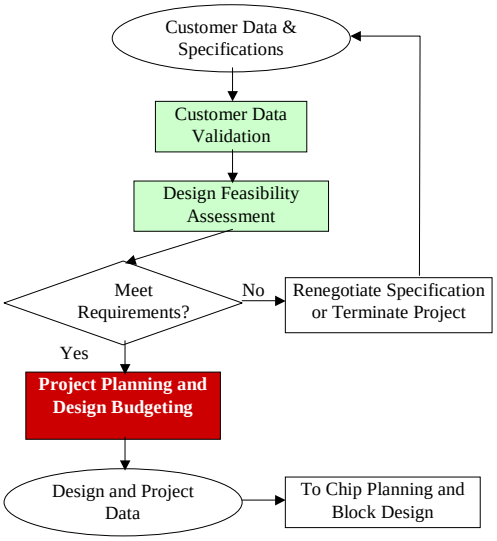
21

Chip Assessment Process



22

Front End Acceptance Flow



23

Project Planning and Design Budgeting

- Develop detailed plans
  - Project schedule (precedence/dependencies, work breakdown)
  - Human resources
  - Machine resources
  - Cost/expenses

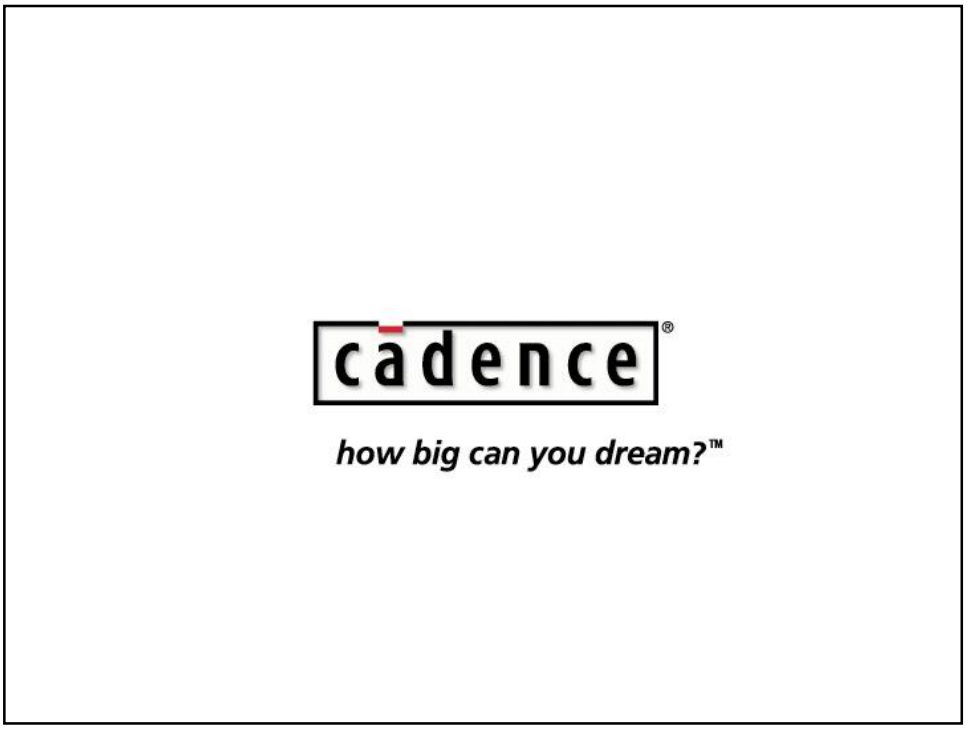
24

Customer Sign-off

- Review and agree on program commitments
- Separation of customer/chip design team responsibilities
- Block acquisition plan
  - Licensing fees, royalties, etc.
- Risks assessment
- Intellectual property rights and protection
- Payment schedule

Conclusions

- Identify any risks associated with trying to meet critical design constraints
- Enable to share risk with the customer where appropriate
- Allow better prediction of cost/performance/etc.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