Evolving ASIC Methodology to Adapt to Technology and EDA Tool Advances

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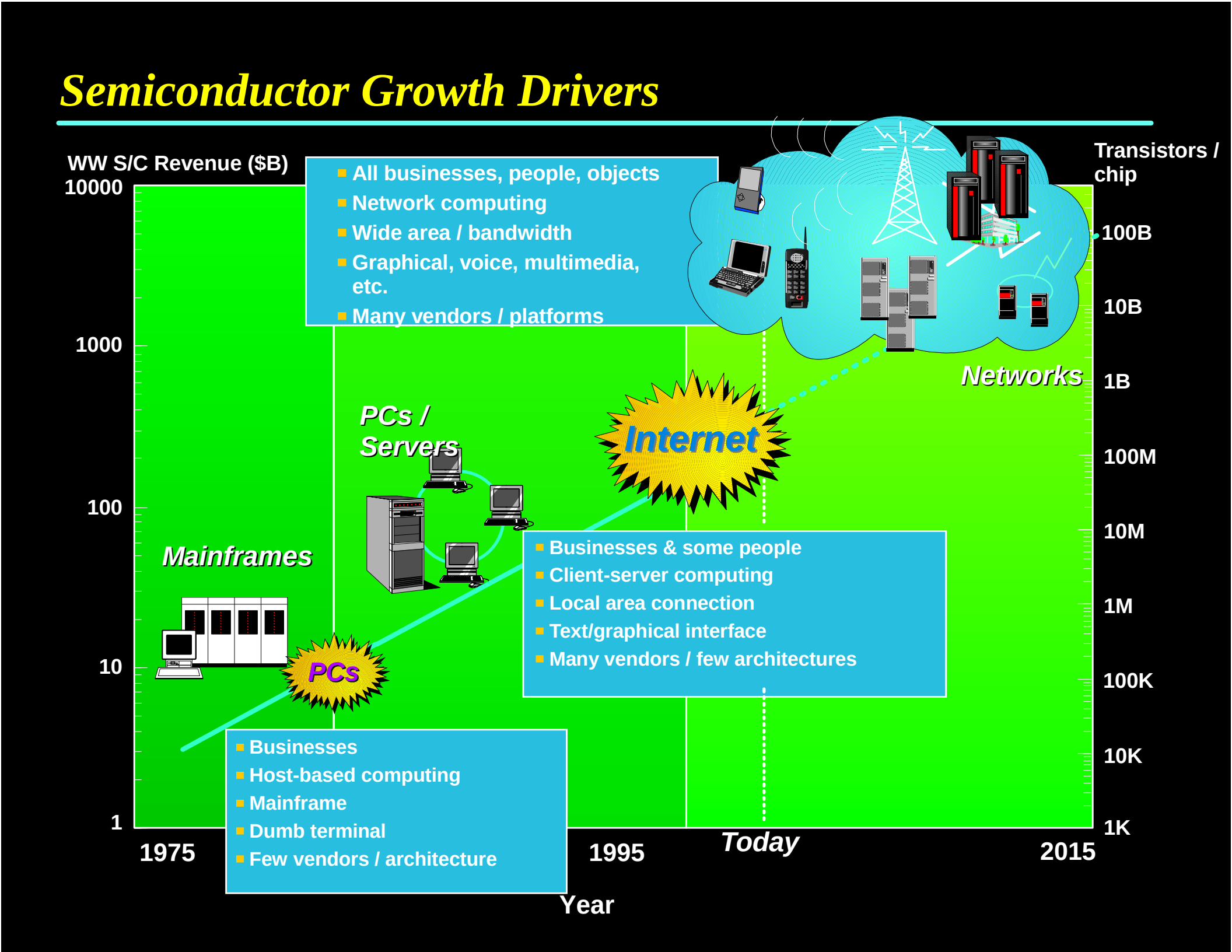
Agenda

- Technology Advances
- Emerging Challenges
- Design Tool Advances
- ASIC Design Methodology Implications
- Conclusion

Semiconductor Growth Drivers



Technology Drivers

- Cost
- High Frequency
- Bandwidth
- Memory
- Power
- Time to Market

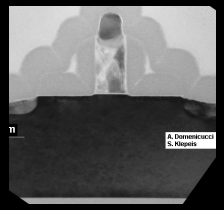
Phones, PDA's, Smart Clothes...

Computers, Net Storage

Routers, Hubs, Switches...

Technology Leadership

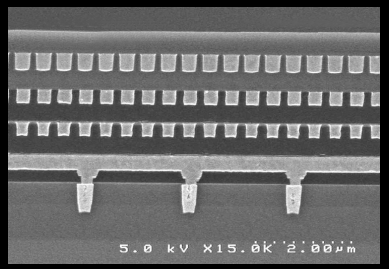
Device Technology



Bulk & SOI CMOS
< 50 nm gates

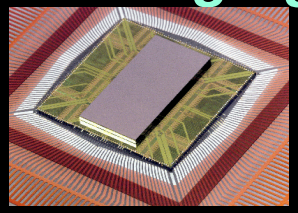
SiGe
BiCMOS
>200ghz

Interconnects



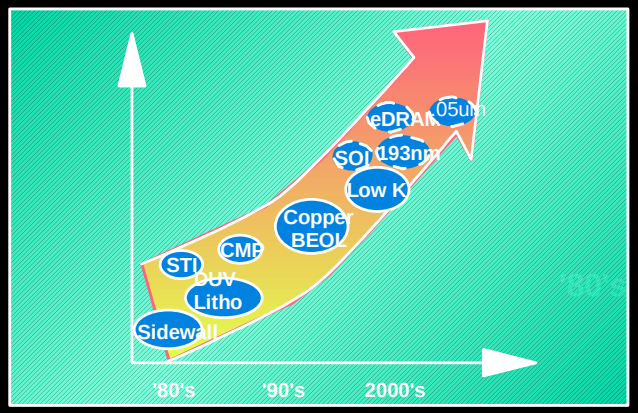
Copper

Packaging

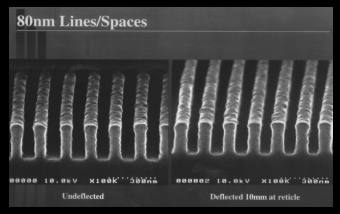


Chip on Chip,
Solder
Bumps, MCM
(polymer
& Ceramic)

Construction Material Changes

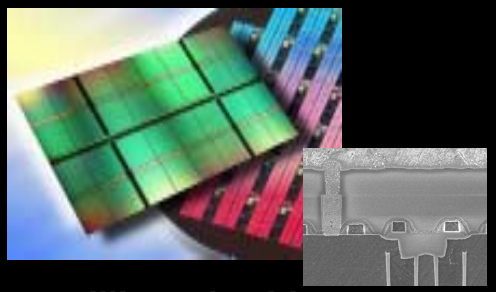


Lithography



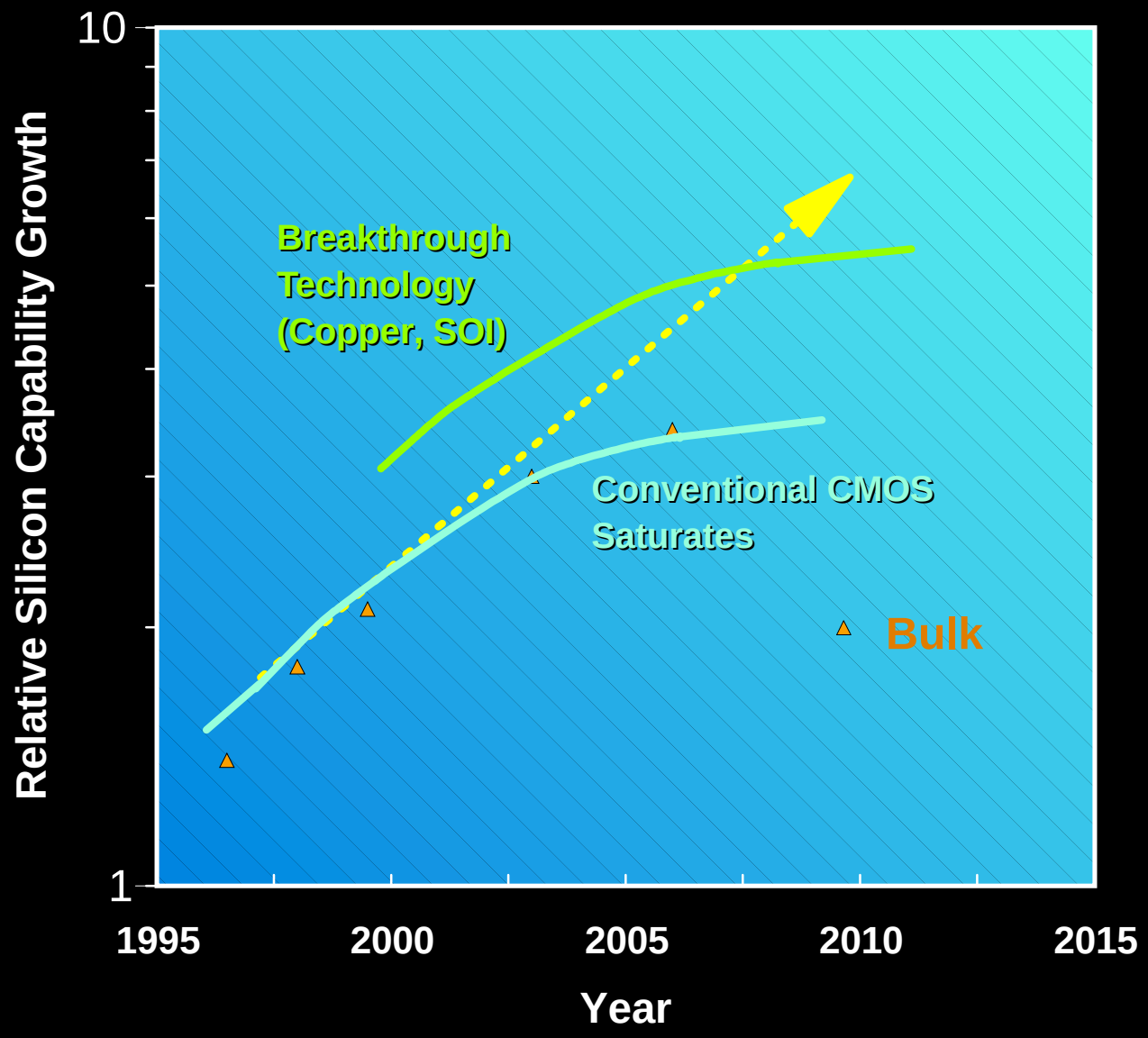
Deep UV, eBeam

Memory

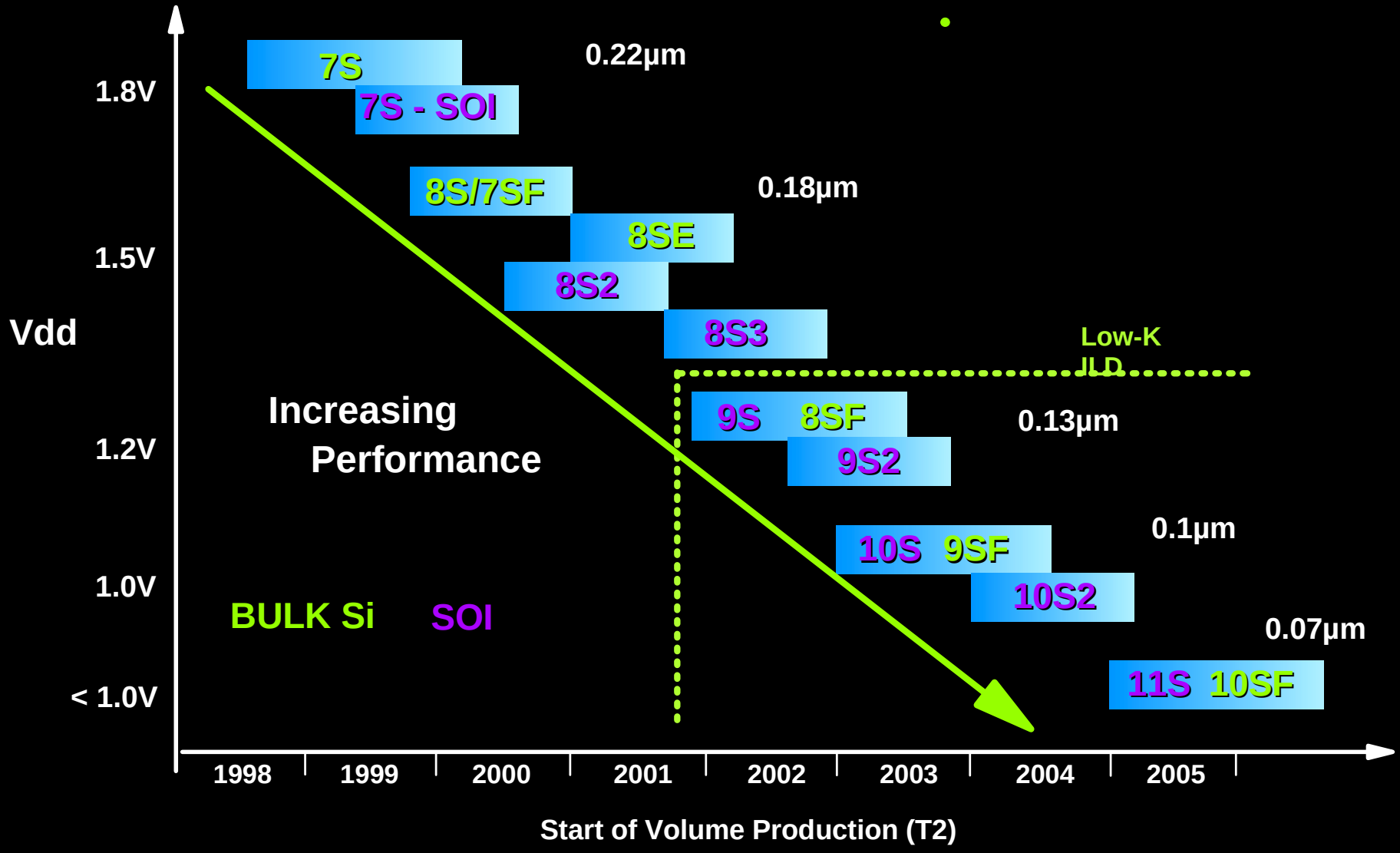


1 Billion Bit Chip,
eDRAM

Require new materials to continue the pace of performance gains



Technology Generation Every 18 - 24 Months



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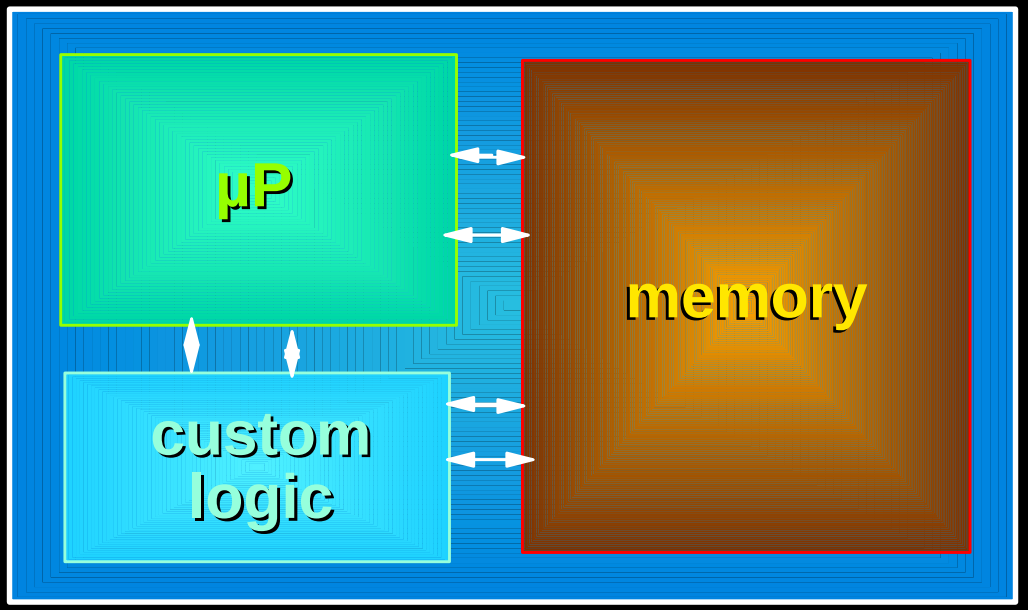
Low-Power Systems

Various sleep modes
- clock gating
- disabling sub-elements
- disable entire µP

Tradeoff power and performance



Multi-voltage operation
- "power down" non critical circuits
- "power-off" circuits while retaining state
  - Control parasitics for lowest leakage
  - Circuit design for low voltage, data retention state
  - Higher voltage operation for read/write

Low-Power Systems

* Power Tradeoffs Best Made during Architectural Design Phase

  - System Issue - Performance, Power, Area
  - Requires functional understanding of design
  - More leverage than late analysis and fix-up
  - Faster tradeoff iteration at higher abstraction

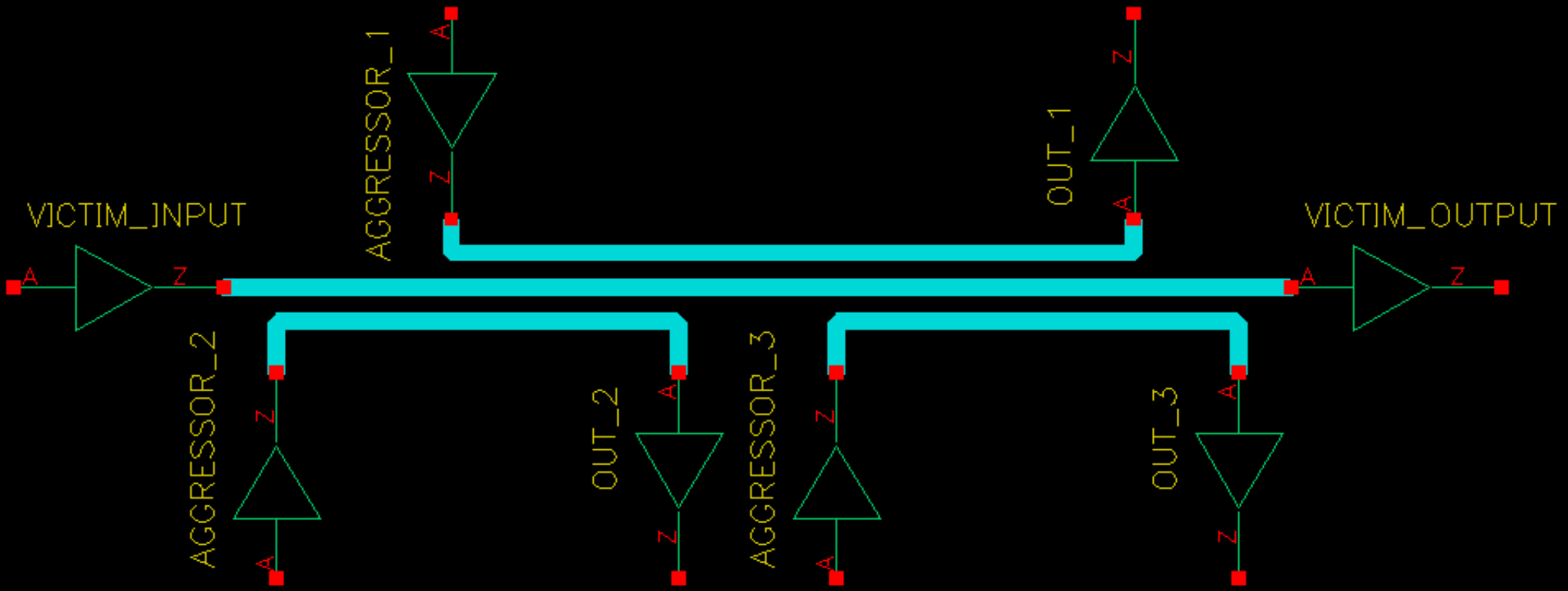
  . . . but must have access to technology feature set
  (multi-threshold libraries, voltage islands etc.)

* Early Power Analysis Requires Improved Modeling Accuracy

  - Technology-specific models for timing accuracy
  - Ability to evaluate multiple operating conditions quickly

Solution involves technology, education, tools, and methodology

Signal Integrity and Noise



Coupled Noise

- "Aggressor" nets couple signals into "victim" nets
- Coupling primarily due to line-to-line capacitance
- Example shows three aggressors and one victim (A-V-A)
- Many other configurations possible over multiple metal levels

Signal Integrity and Noise

* Noise is a progressively worsening problem as geometries shrink

* Could become a gate to customer "first time right" success

* Noise is a complex, multifaceted problem
    - Statistical phenomenon
    - Several types: coupled, supply, substrate
    - Layered approach required to address each type

*Solution involves education, design, tools, and methodology

* Objective is to reduce the probability of a design failure while minimizing impact to design TAT, performance, and density

Signal Integrity and Noise

* Noise is not a new problem - faced by I/O designers for 20+ years

* May cause false switching or timing fails

* Evolved / evolving into an on-chip problem

* Aggravated by many issues:

  - Faster chips -> higher edge rates, less Dt tolerance
  - Higher edge rates -> more coupled and supply noise
  - Lower Vdd -> lower noise immunity
  - Wire scaling -> more R, more capacitive coupling (Ccoupled/Ctotal)
  - Constant power @ lower Vdd -> more I -> more I-R loss
  - Higher I/O Vdd supplies -> increased coupled noise
  - Increasing substrate currents -> more substrate noise

Signal Integrity and Noise

*** Noise is a statistical phenomenon**
Statistical problems can be significantly reduced but not fully eliminated

*** Noise reduction can be costly if done without finesse**
Design TAT, performance and density impacts

- **"How can I fix 40,000 failing nets?"**
- **"Why did my critical path slow down by 40%?"**

*** Noise avoidance as important as noise analysis**

- **Limit size of remaining problem to analyze**
- **Limit number of nets to repair**

Noise avoidance via education, design, tools, and methodology

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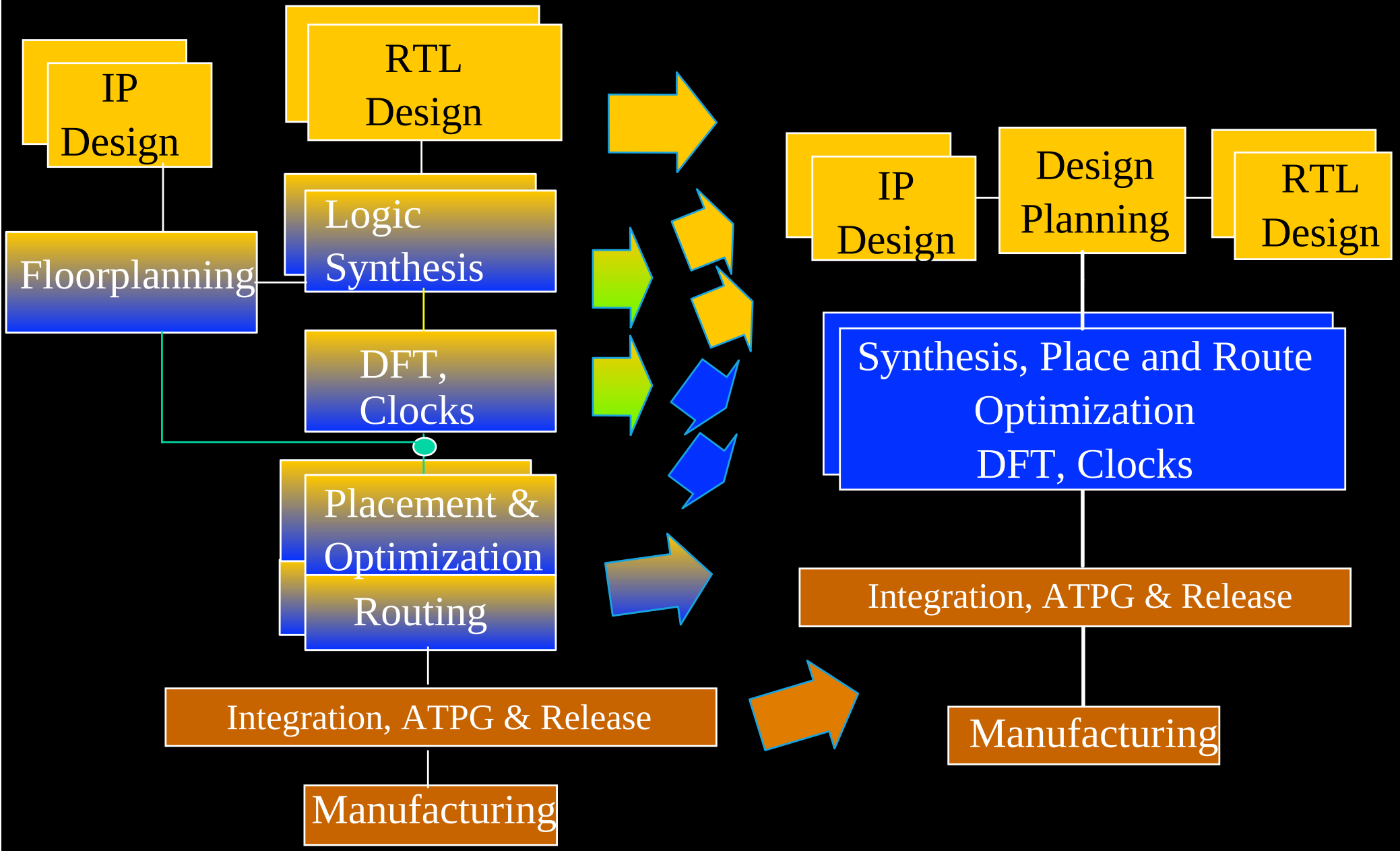
ASIC Design Tool Evolution



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Design Methodology Must Evolve

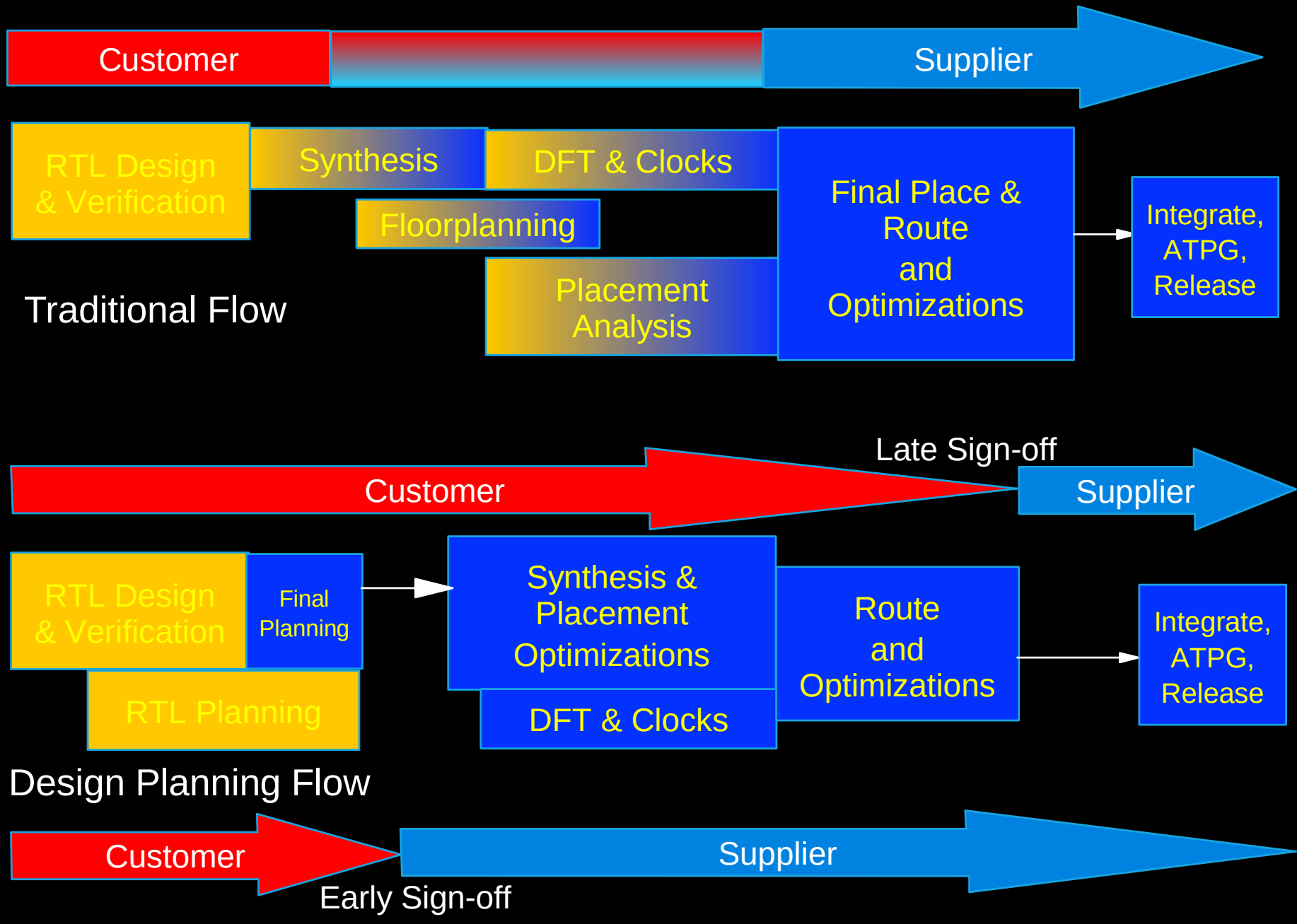
★ To Enable Access to Technology Features

- Early, Architectural-Stage Vision is Essential
  - Modeling must be evermore accurate in predicting ultimate results
  - Tool execution must be fast to enable iteration
  - Issues resolved early yield enormous TAT benefits

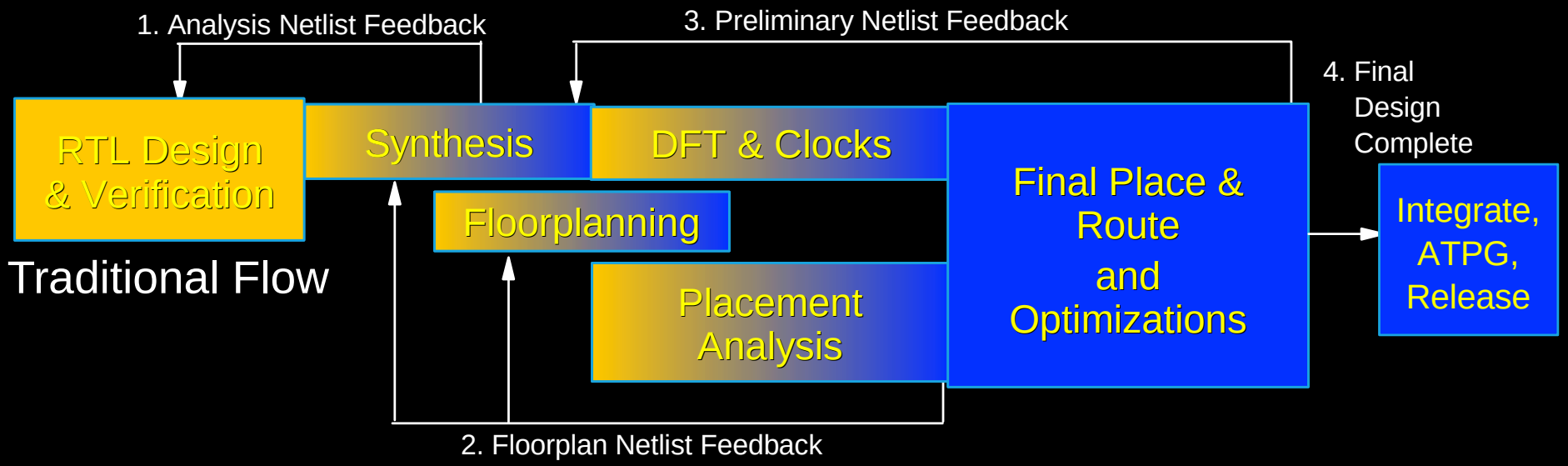
★ To Efficiently Employ New-Generation Design Tools

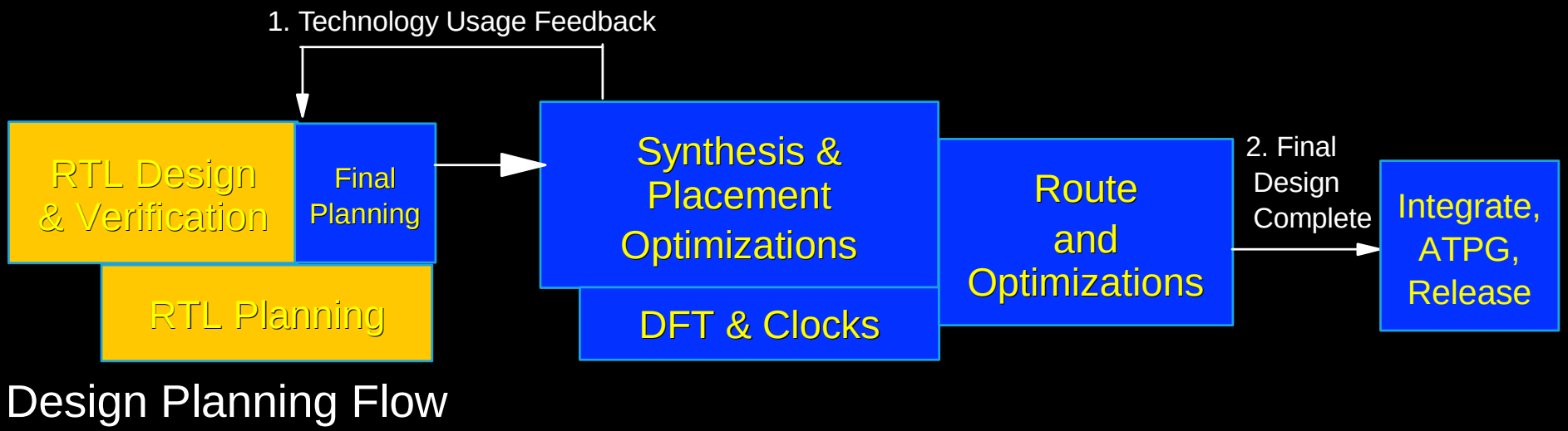
- Integrated Synthesis, Placement
  - Dictates "Same Seat" execution of synthesis and placement steps
  - Sign-off point must move to accommodate
- Advent of Design Planning Tools
  - Enables Early Focus on Technology Features
    - Performance, Power, Area, Testability, Cost, Signal Integrity
  - Key to Accelerating ASIC Turn-around-time

New Design Methodology: Two Engagement Models



New Design Methodology: Efficient and Precise





Modeling Dependencies of the New Methodology

- **Model Accuracy is More Important than Ever**
  - For Early Design Planning:
    - Models must enable fast tradeoff experimentation
      - Must provide visibility into power, timing, area vs. environment, process
    - Models must enable accurate prediction of downstream results
    - High-Level Abstraction path
      - Required accuracy with optimal runtime
  - For Detailed Design:
    - Model accuracy must approach 100% precision to overcome pessimism
    - Accuracy guaranteed by silicon supplier

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ASIC Methodology 2002

★ ***ASIC Methodology is Evolving to Support Technology and Tool Advances***

★ ***Signoff Model moving In "both directions"***

- Early Signoff
  - ASIC Supplier Handles Silicon Details
  - Customer Focus on Function
- Late Signoff
  - Customer Owns Both Function and Silicon Implementation

★ ***There will be ASIC Customers for Both Engagement Models***