Platform Based Design:

Report from the Front

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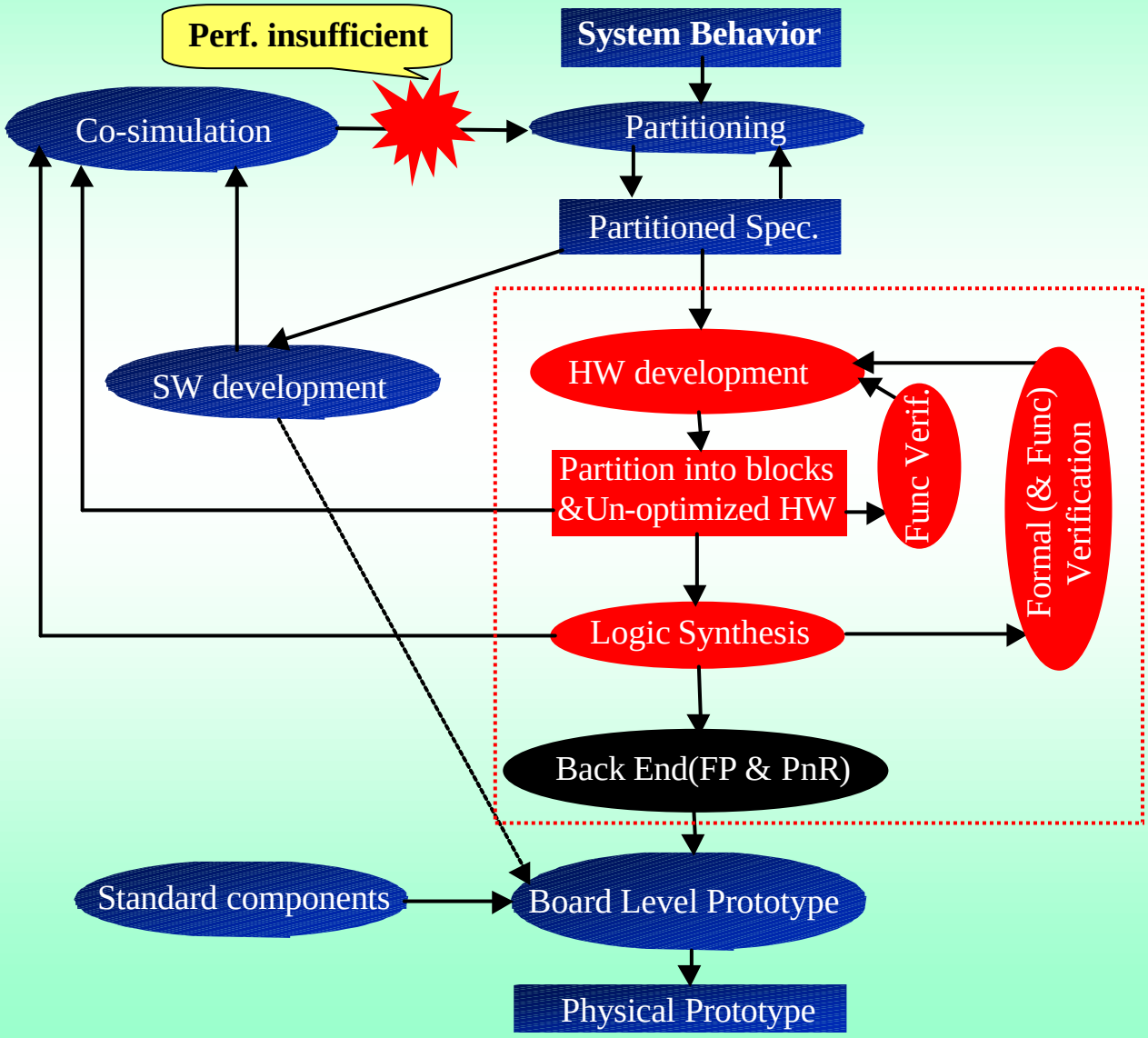
Presentation Topics

- Introduction: Embedded System design flow
- Need of a higher level of abstraction of hw
- HW Design Platform
- TriCore based design platform
  - Platform details
  - Configurability of hardmacro of uP, Memories, & Busses
- Results: SoCs based on TriCore
- Conclusion

Embedded System (or HW/SW co-) Design Flow - A Simple view



HW components of an Embedded Sys.

- **Embedded Systems are implemented as mixed sw-hw systems. SW is, generally, used for features and flexibility, and HW is used for performance {e.g. Cameras, cellphones, industrial controllers, etc.}.**

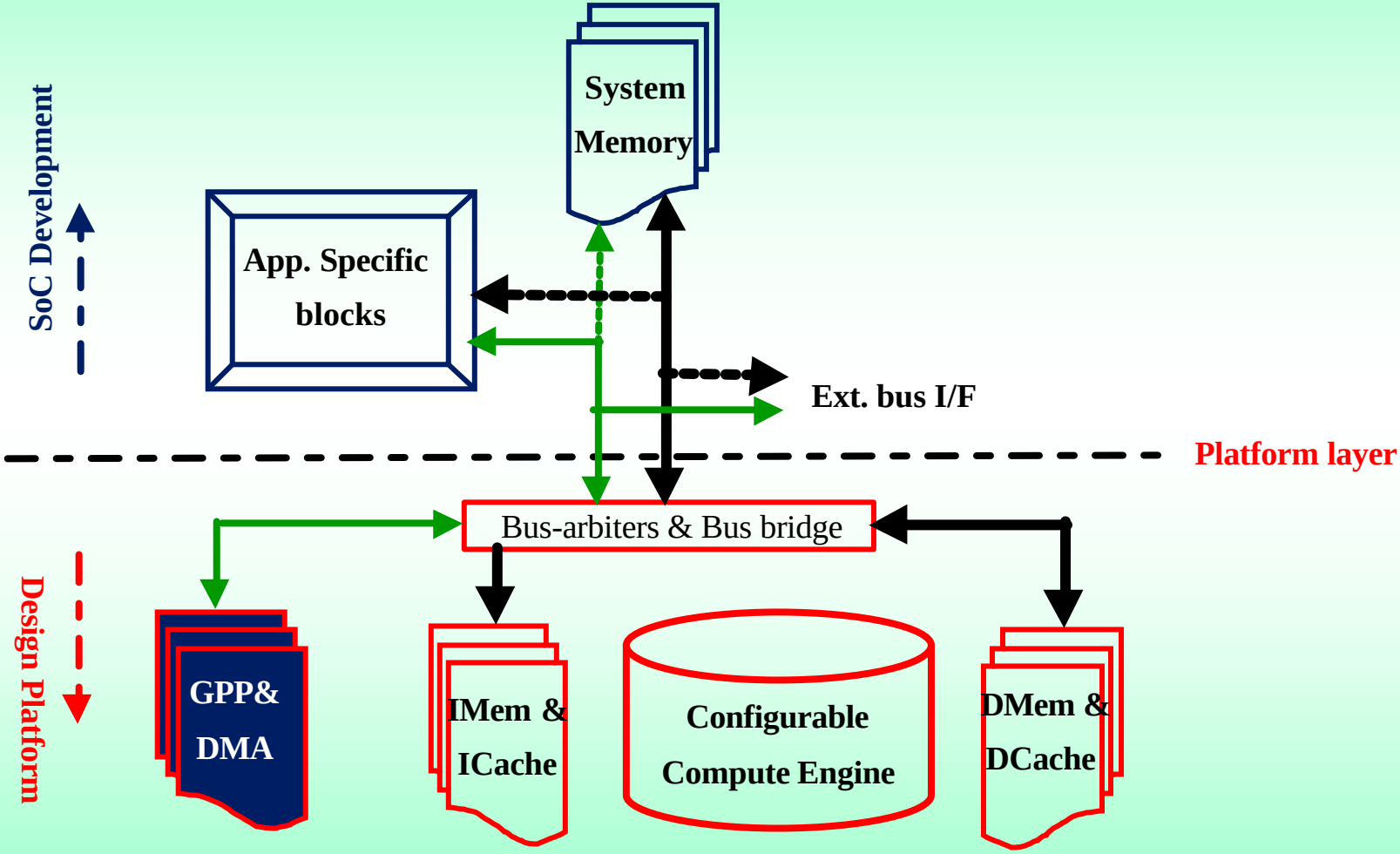
- **Compute Engine: Microcontroller, uP/uC (RISC), DSP**
- **Program and Data Cache/Memories (Varying Size)**
- **One or more Buss-Interconnects**
- **Application specific HW**
- **DMA, Interrupt support**
- **General Purpose Peripherals**

HW components of an Embedded Sys.

- **General Purpose Peripherals (GPP):**

  - **–ASC: Async./Sync. Serial Interface**
  - **–SSC: High Speed Synch. Serial Control**
  - **– UART: Universal Asynchronous Rx/Tx**
  - **–IIC: Inter-Integrated Circuit, Serial Bus**
  - **–RTC: Real Time Clock**
  - **–STM: System Timer**
  - **–GPTU: 3x 32-bit General Purpose Timers**
  - **–GPIO: Up to 64 General Purpose I/O**
  - **–WDT: Watch Dog Timer**
  - **– …. etc.**

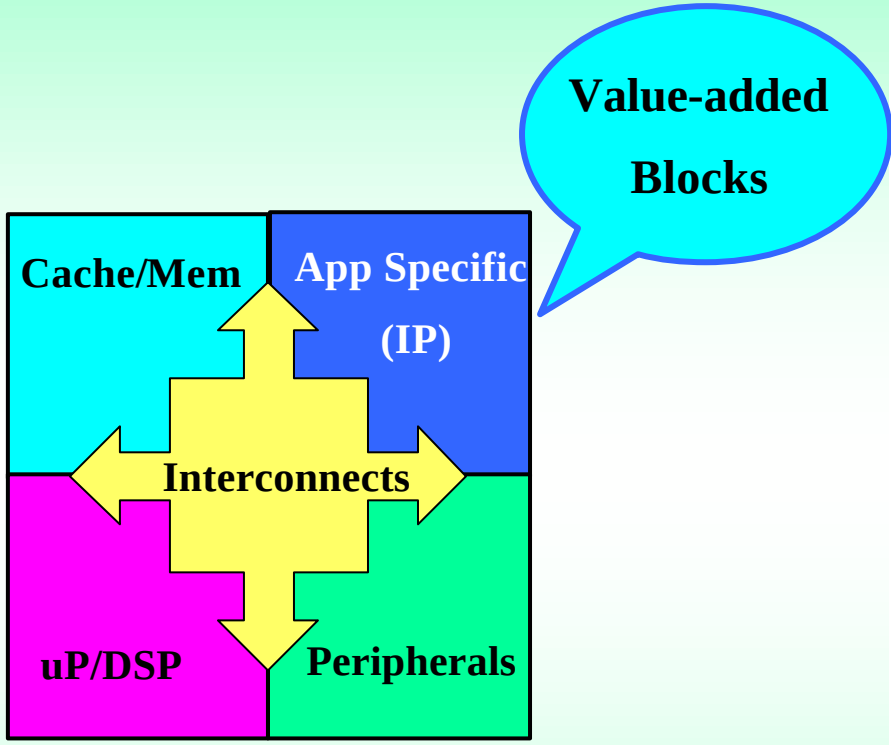
HW Design Platform



HW Design Platform (cont..)

From the platform (GUI or HDL):

- **RISC @200Mhz worst,250MIPs**
- **DSP @200 Mhz worst, 300MMs**
- **IMem (32KB), Icache(16KB)**
- **DMem(32 KB), Dcache(16KB)**
- **GPPs (ASC,RTC,I2C,STM,GPT,GIO)**
- **DMA, & Interrupt service**



Develop HDL:

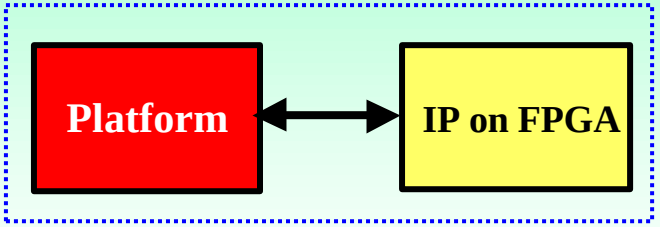
- **Application specific blocks**
- **System Memory (compiler generated)**
- **Top level interconnect signal hook-up.**

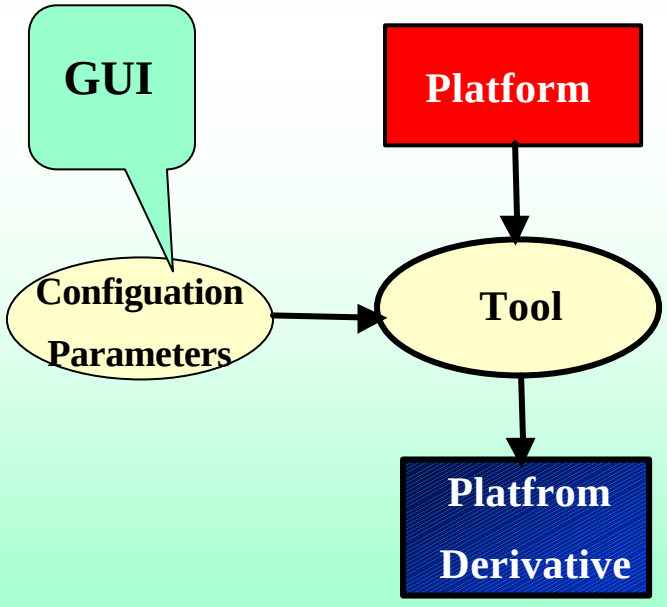
Platform Deliverables

- RTL with synthesis scripts (For soft-macro)
- Timing shell, Timing Analysis scripts, Backend views (For Hardmacro)
- Bus Function models for bus interconnects
- High level compute-engine model
  - ISS and/or Cycle-Accurate
- High level models for GPPs
- Verification environment/methodology
- Basic Software
  - Boot code, basic handler, test-programs*, Tests vectors
  - RTOS

Platform Deliverables (optional)

- **Emulation**
  - **FPGA-portable or**
  - **Platform-chip**
- **Performance Evaluation & Analysis Support (sw/hw)**
  - **Cache hit/miss rates**
  - **MMU Pages hit/miss rate**
  - **Communication traffic (i.e. bus utilization)**
  - **Memory traffic**
  - **Interrupt rate & response time**
- **Configuration Tools**





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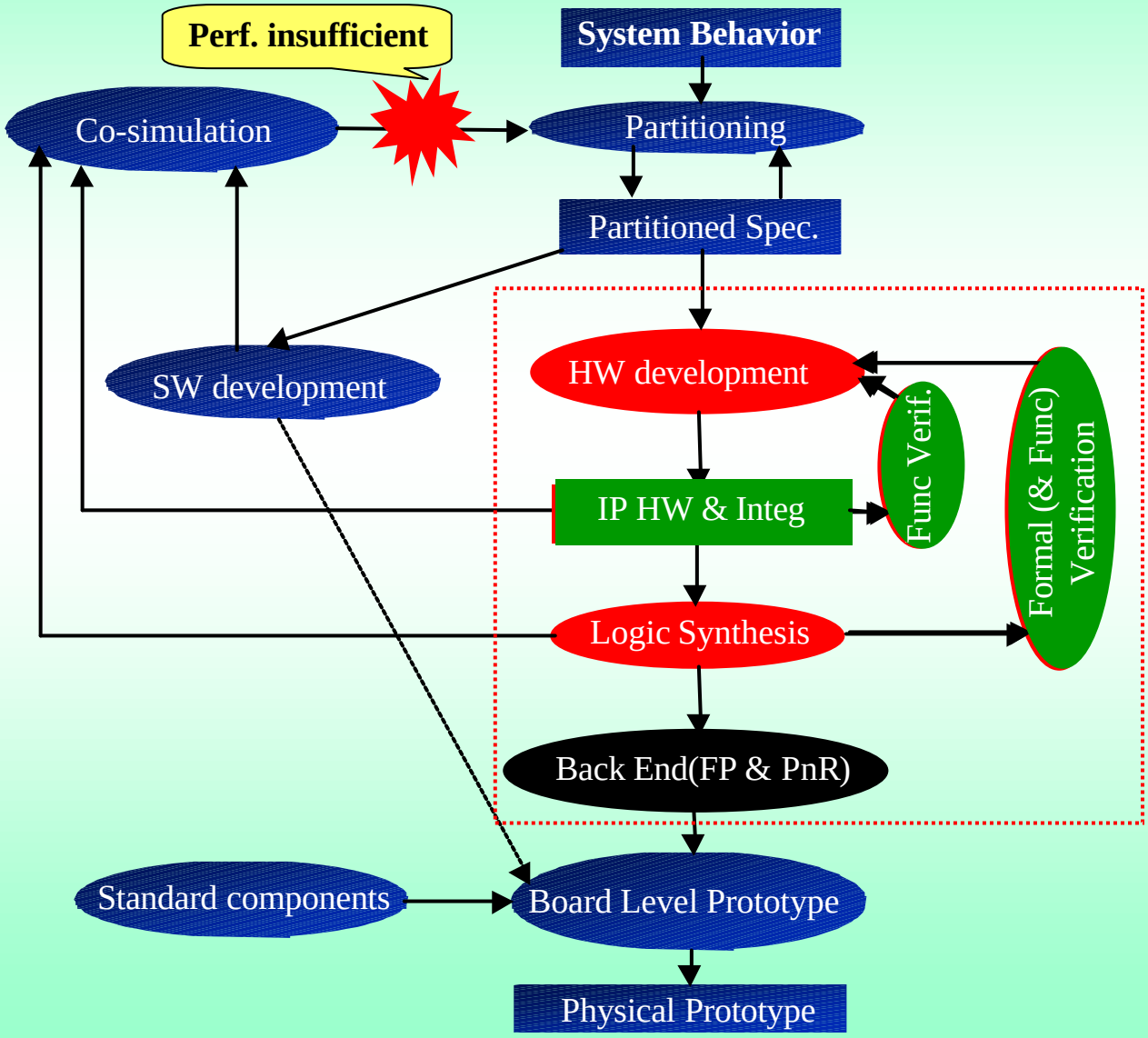
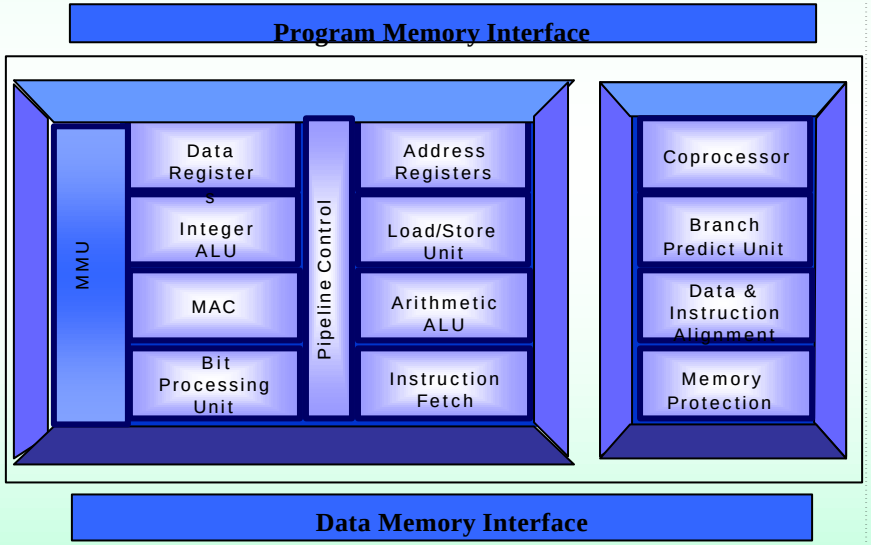
Embedded System (or HW/SW co-) Design Flow with Design Platform



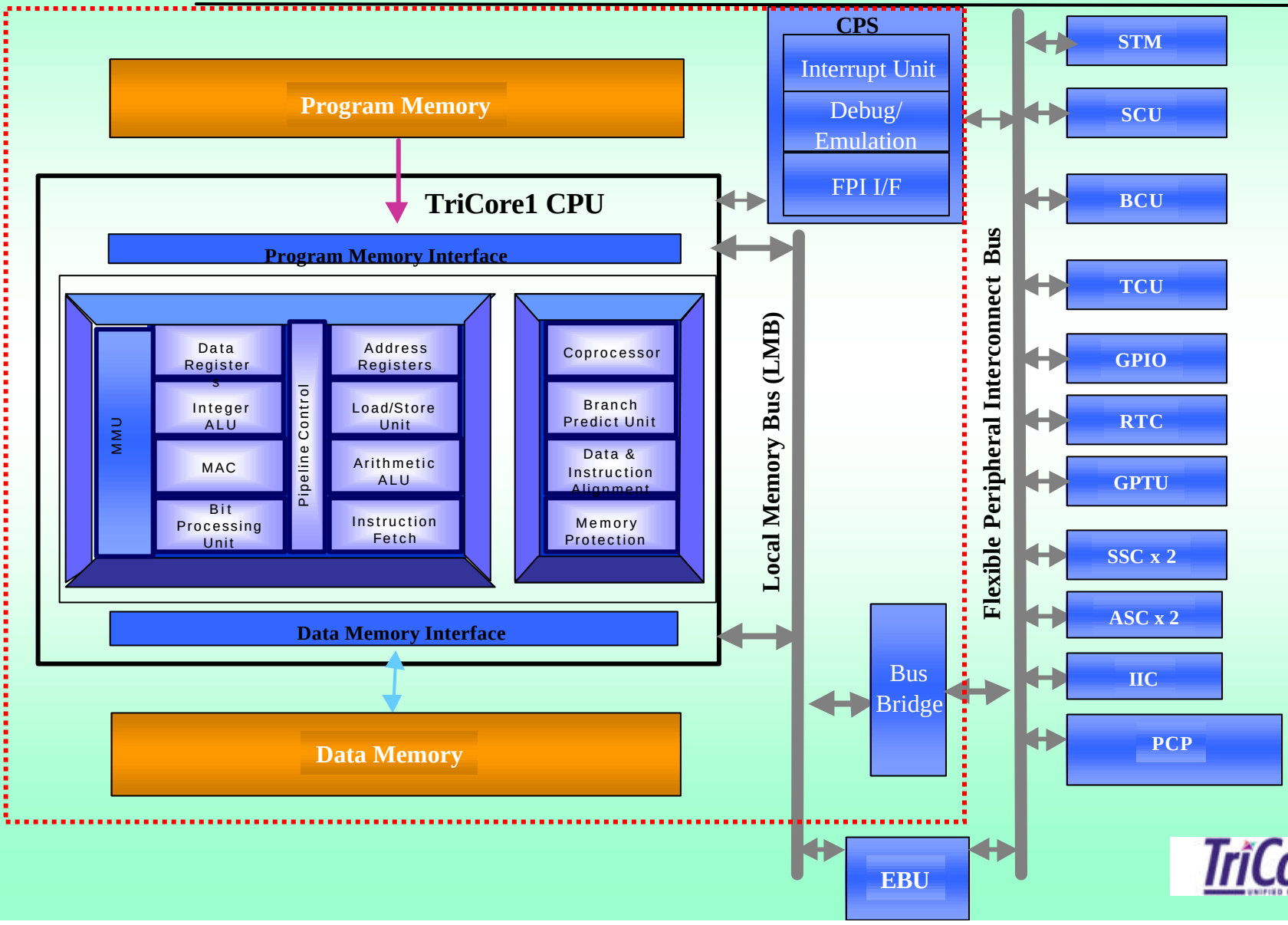
TriCore - TC1 Architecture Overview

- 32-bit Unified RISC+DSP
- Load/Store Architecture
- HW controlled context saving
- Fast context switch (shadow registers)
- Fast interrupt response (~6 clocks)
- Superscalar: Three pipelines
- Zero Overhead loop
- 16-bit / 32-bit Instruction Format
- Single-cycle dual MAC
  - 32x32, 16x32, Dual 16x16
- On-Chip debug support
- MMU, COP
- TC1 (300Mhz, typ, 0.18u), TC2 (600Mhz,typ, 0.13u)

TC1 CPU



TriCore1 SOC Platform - TCSOC

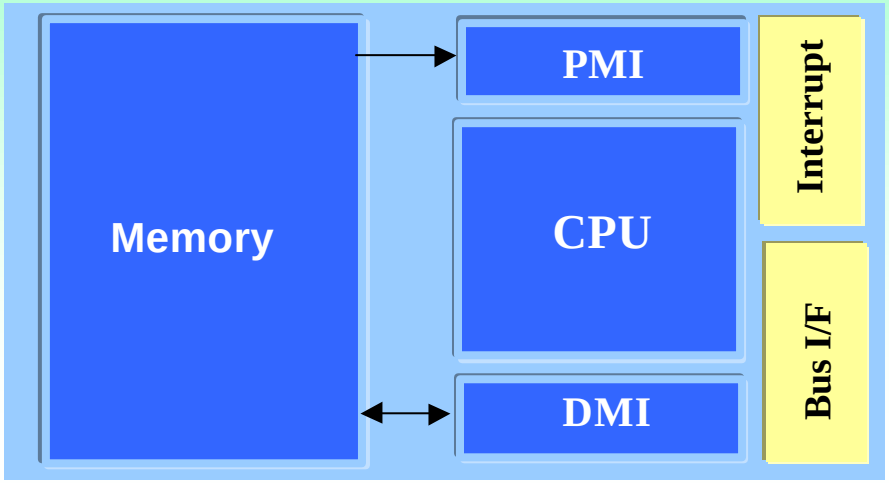


TCSOC: Compute Engine,TriCore1

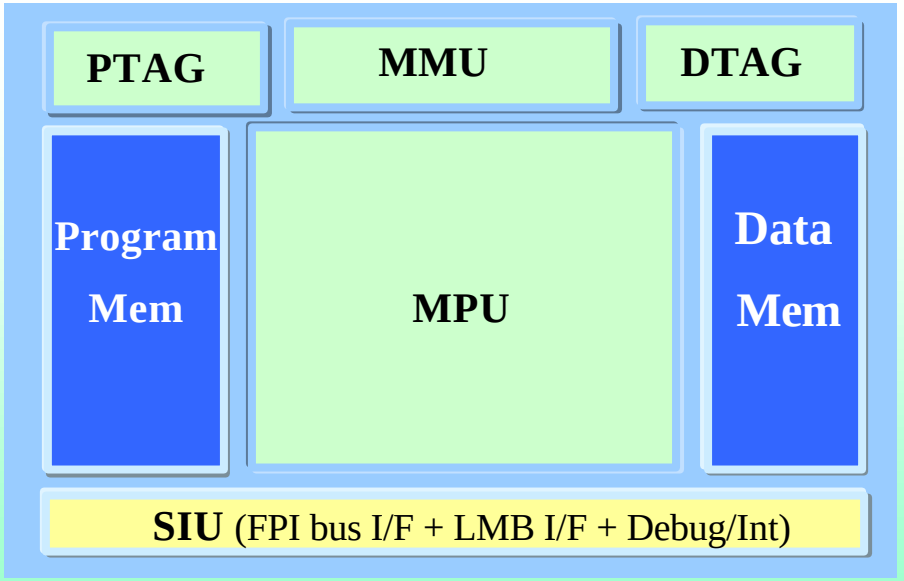
- TriCore1 Microprocessor System (MPS)
  - Configurable Program & Data Cache/Memory I/F
  - optional MMU and FPU.
- PCP : 32-bit Peripheral Control Processor Processor
- 64 (low latency) & 32 bit busses
- Set of System- and General Purpose Peripherals:
  - ASC: Async./Sync. Serial Interface
  - IIC: Two channel I2C Serial Bus
  - RTC: Real Time Clock
  - SSC: High Speed Synch. Serial Control (SPI-compatible)
  - STM: System Timer
  - GPTU: 3x 32-bit General Purpose Timers
  - GPIO: Customizable General Purpose I/O
  - EBU: External Bus Interface for Off-Chip Memory
  - Test Control Unit (OCDS & JTAG I/F)
  - System Control Unit (Reset Control, Power Management,Watch Dog Timer)

TCSOC: Design & Arch considerations

- **Partitioning based on functionality**



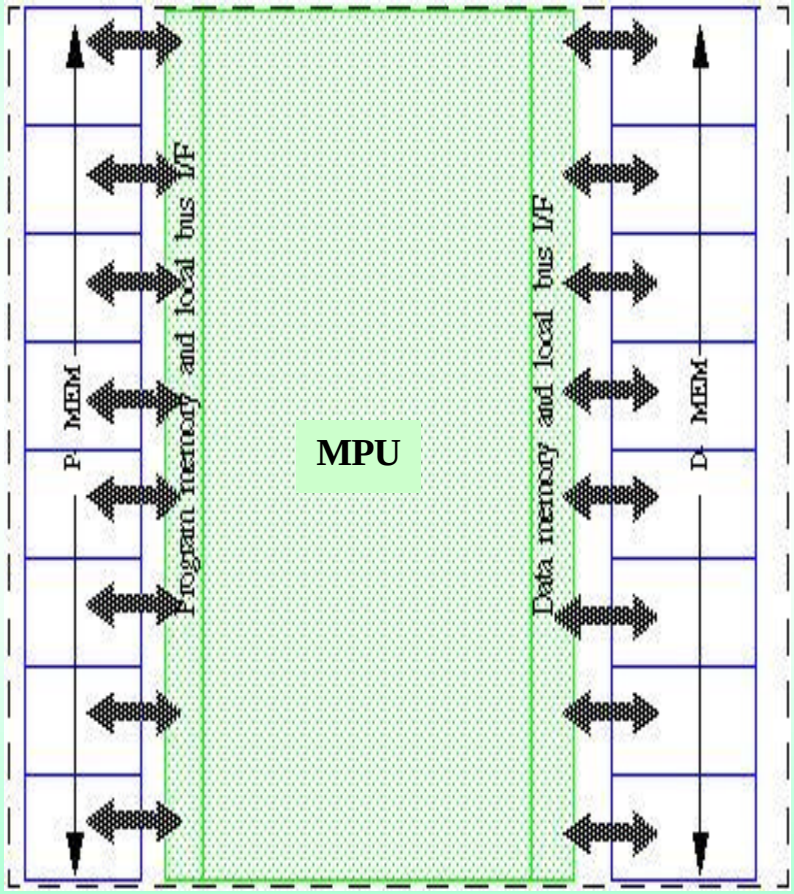
- **Partitioning based on reusability**



Design & Arch considerations (II)

Code/Data Memories

- Configurable selection between mem & cache
- All pins abutt w/o routing
- eight block on either side



TCSOC: Bus Interconnects (LMB & FPI)

- TC1 MPS : TriCore1 Microprocessor System
  - Configurable Program & Data Cache/Memory I/F
  - optional MMU and FPU.
- PCP : 32-bit Peripheral Control Processor
- 64 (low latency) LBM, & 32 bit FPI
- Set of System- and General Purpose Peripherals:
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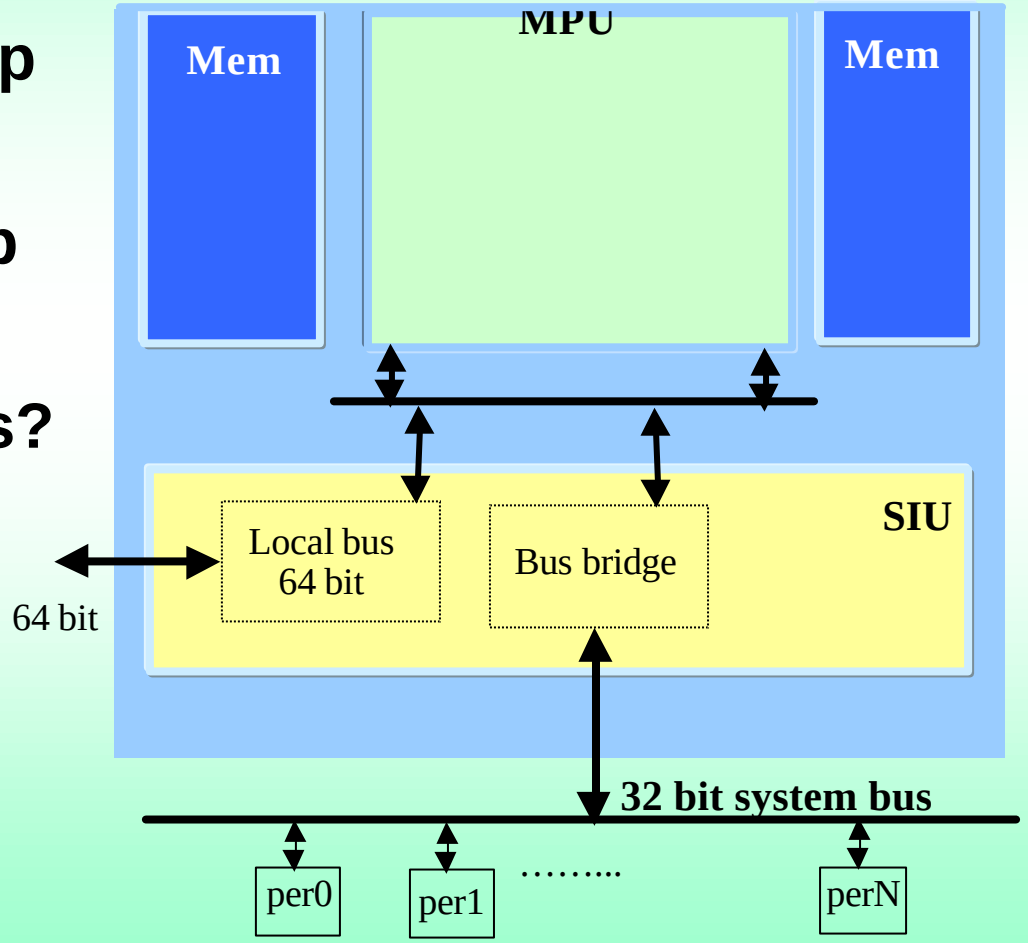
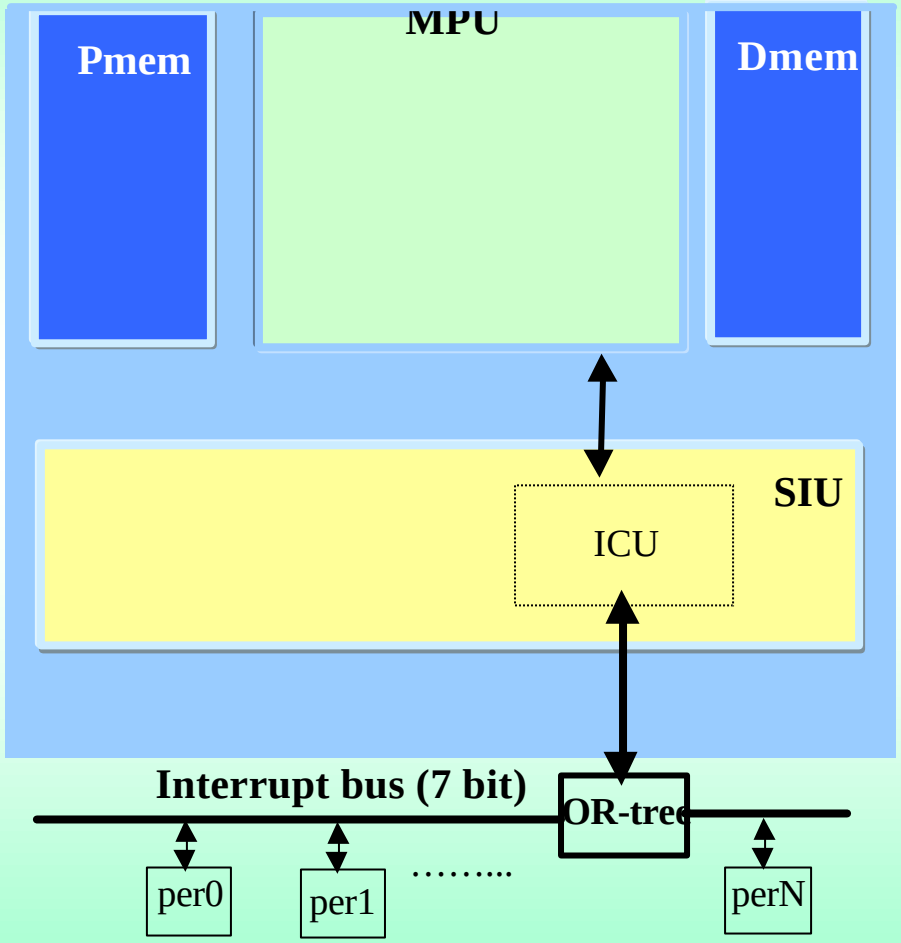
TCSOC: Bus Interconnects (cont..)

- 64 bit on-chip & off-chip bus I/F
- 32 bit on-chip & off-chip bus I/F
- Large no. of peripherals?
- System bus & cpu freq ratio 1:1, 1:2, …, 1:n
  - Signal configurable

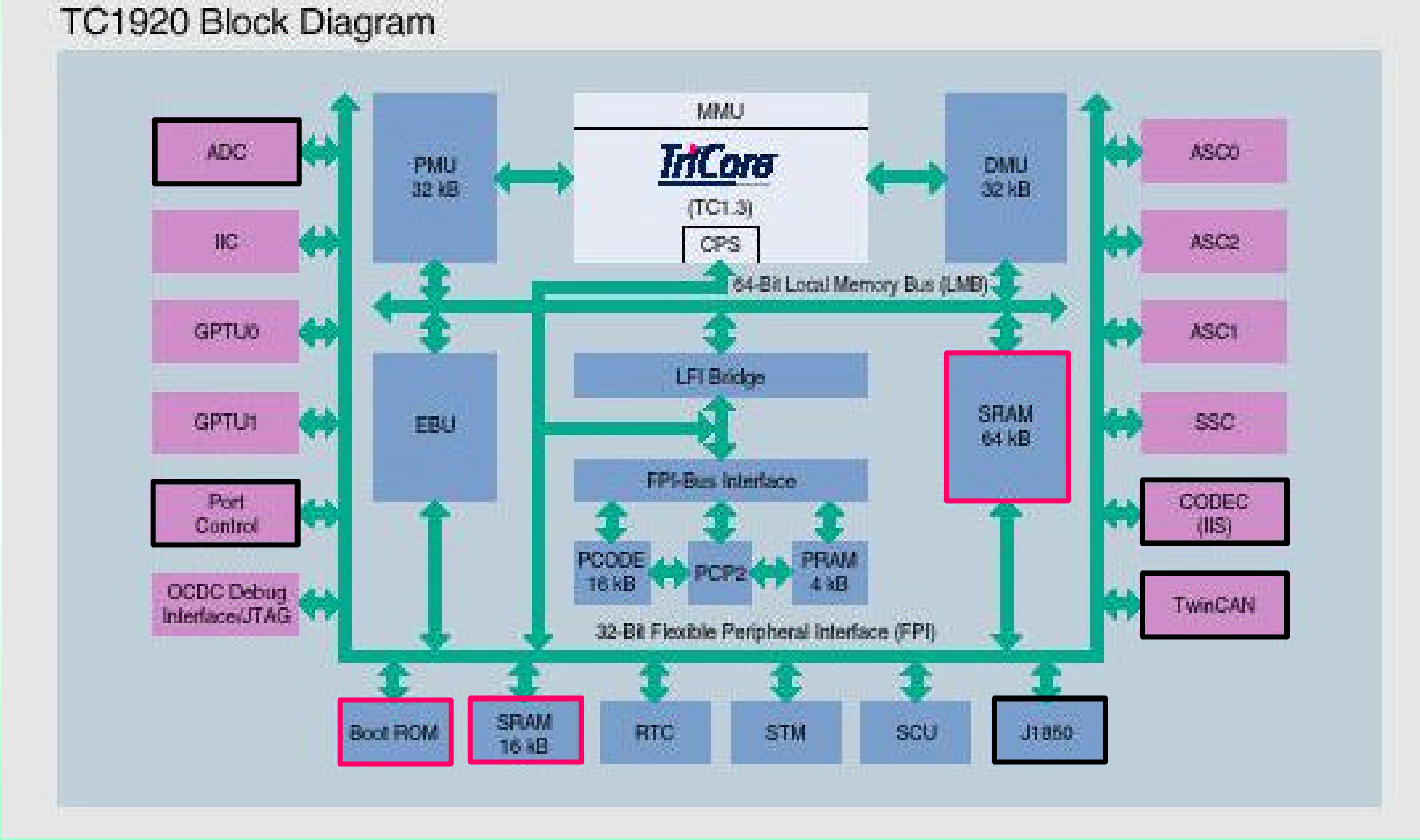


TCSOC: Interrupt System

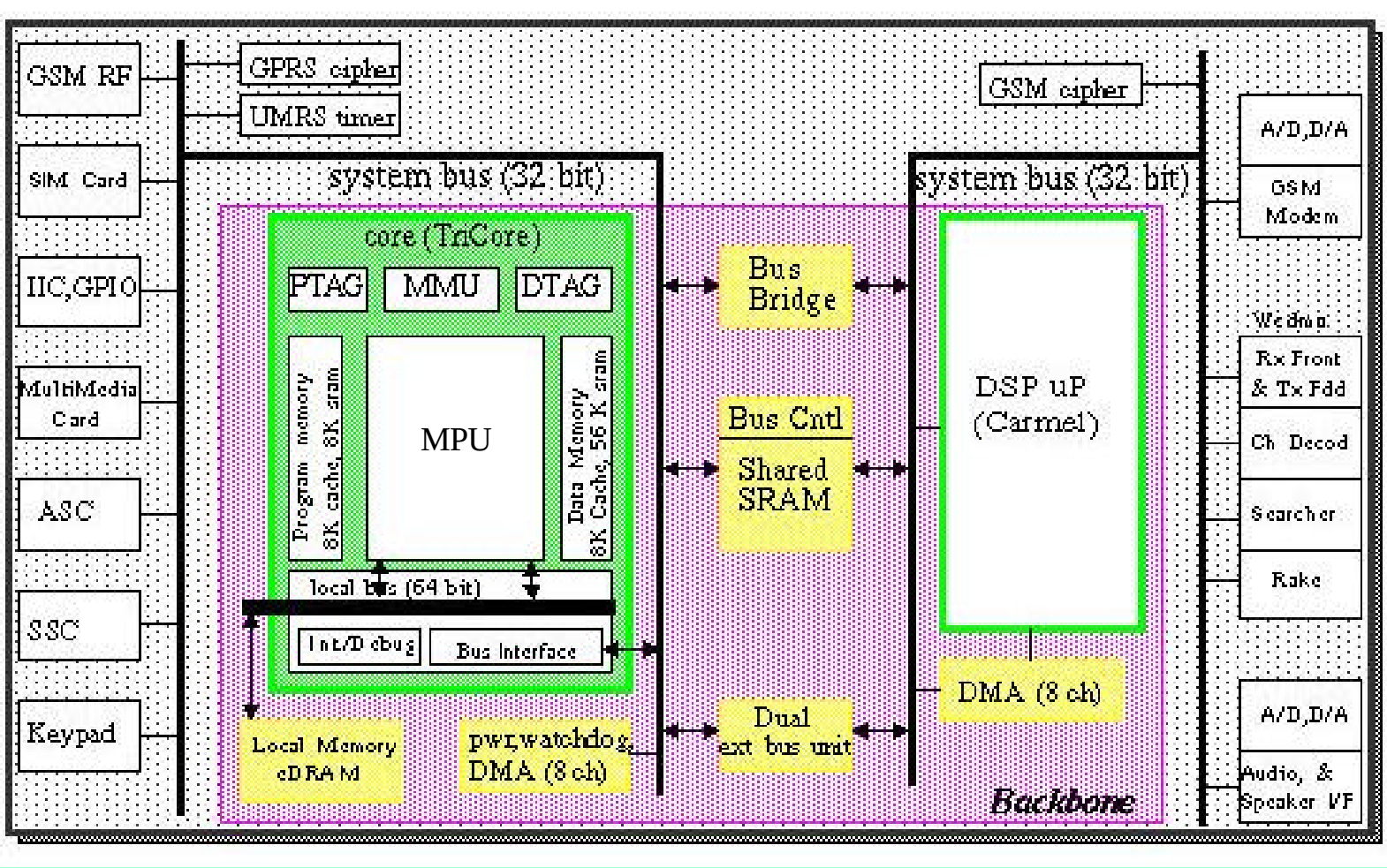
- **Independent Interrupt Control Unit**
- **255 interrupts, connected with 7bit arbitration bus**
- **ICU freq ratio 1:1, 1:2, …, 1:n**
  - Signal configurable
- **Interrupt bus cycle 1 or 2 of CPU clock cycle**
  - Register configurable



Telematics Controller – TC1920



Triple-Mode Baseband IC



Conclusion

Design Platform:

- High-performance configurable RISC/DSP
- Bus interconnects (at least one low latency)
- General Purpose Peripherals
- PCP, and Interrupt system

By Using Design Platform:

- Quick development of derivative designs (i.e. SoC).
- Designer concentrates on system design rather than components
- Designer uses a proven design methodology

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Never Stop Thinking

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