9th IEEE/DATC Electronic Design Processes Workshop, EDP 2002

SpecC Methodology for High-Level Modeling

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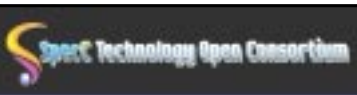
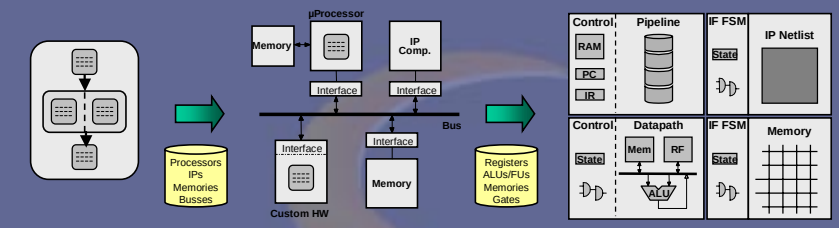
http://www.cecs.uci.edu/~specc/

Outline



- System design
- SpecC design methodology
- Specification model
- Architecture model
- Communication model
- Implementation model
- Summary & conclusions

System-On-Chip Design



Specification + constraints | **System architecture + estimates** | **RTL/IS Implementation + results**

- Specification to architecture to implementation
- Behavior to structure
  1. System level: system specification to system architecture
  2. RT/IS level: component behavior to component microarchitecture

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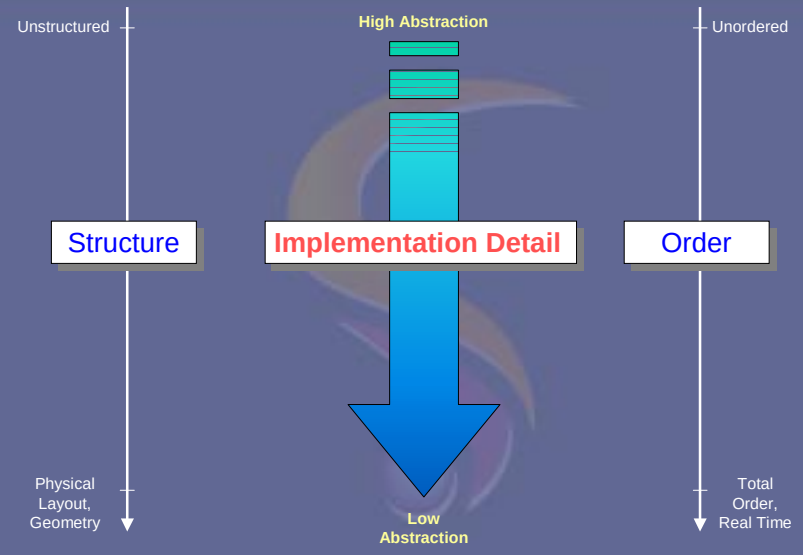
Abstraction Levels



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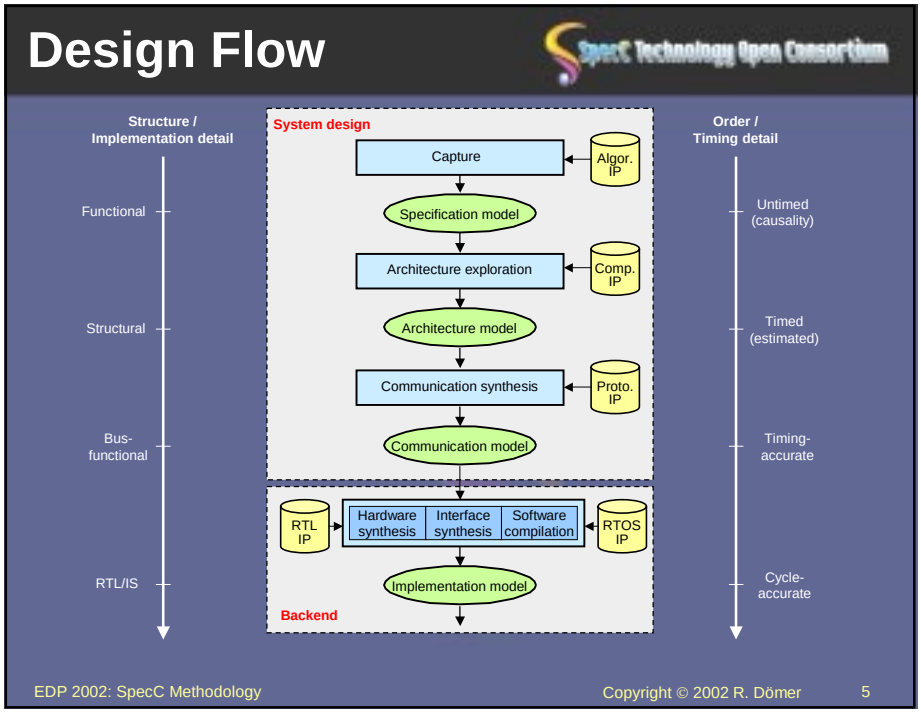
Design Flow
Structure / Implementation detail
Functional
Structural
Bus-functional
RTL/IS
System design
Capture
Algor. IP
Specification model
Architecture exploration
Comp. IP
Architecture model
Communication synthesis
Proto. IP
Communication model
RTL IP
Hardware synthesis
Interface synthesis
Software compilation
RTOS IP
Implementation model
Backend
Order / Timing detail
Untimed (causality)
Timed (estimated)
Timing-accurate
Cycle-accurate
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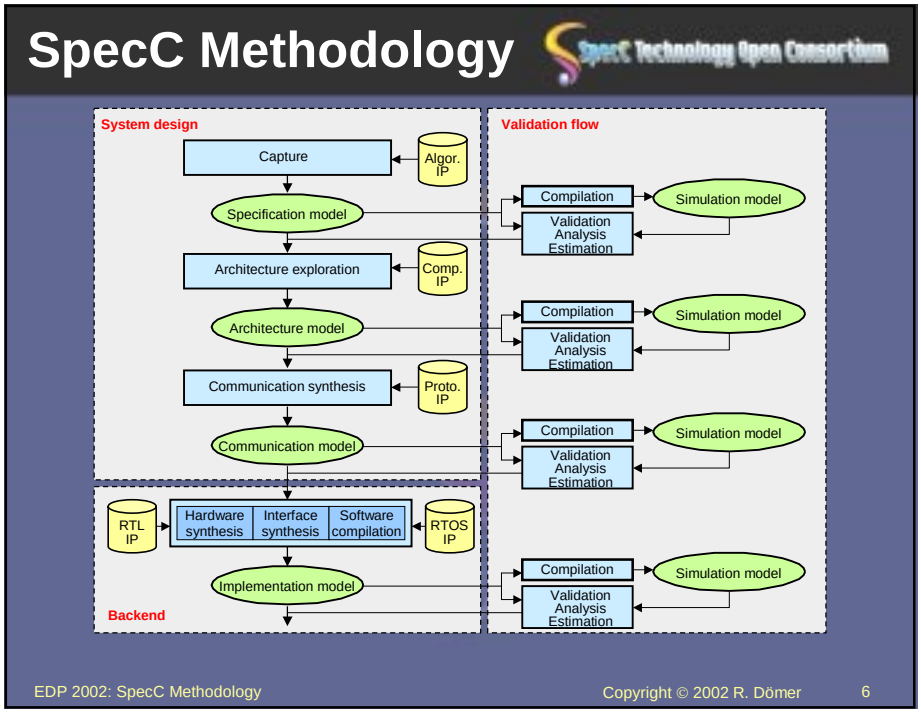
SpecC Methodology
System design
Capture
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Communication synthesis
Proto. IP
Communication model
RTL IP
Hardware synthesis
Interface synthesis
Software compilation
RTOS IP
Implementation model
Backend
Validation flow
Compilation
Validation Analysis Estimation
Simulation model
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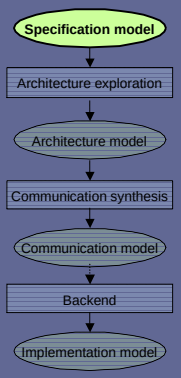
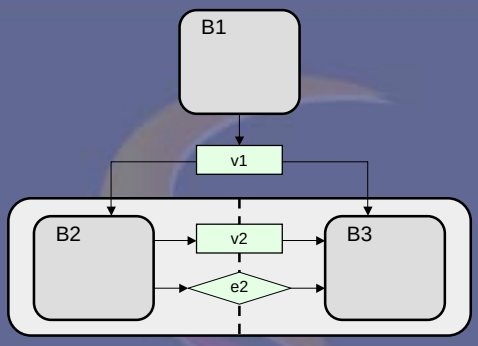
Specification Model

- **High-level, abstract model**
  - Pure system functionality
  - Algorithmic behavior
  - No implementation details
- **No implicit structure / architecture**
  - Behavioral hierarchy
- **Untimed**
  - Executes in zero (logical) time
  - Causal ordering
  - Events only for synchronization



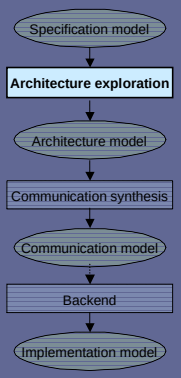
Specification Model Example



- **Simple, typical specification model**
  - Hierarchical parallel-serial composition
  - Communication through ports and variables, events

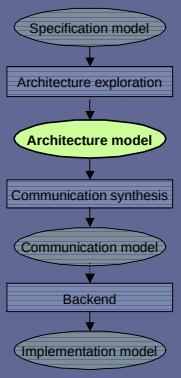
Architecture Exploration

- **Component allocation / selection**
- **Behavior partitioning**
- **Variable partitioning**
- **Scheduling**

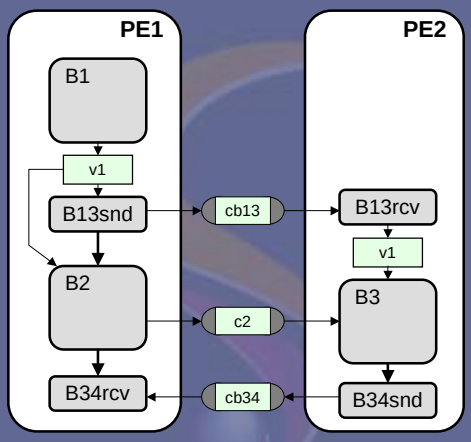


Architecture Model

- **Component structure/architecture**
  - Top level of behavior hierarchy
- **Behavioral/functional component view**
  - Behaviors grouped under top-level component behaviors
  - Sequential behavior execution
- **Timed**
  - Estimated execution delays



Architecture Model Example



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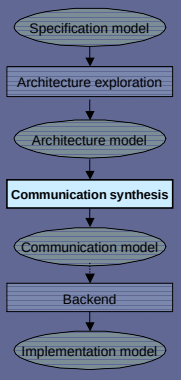
Communication Synthesis

- **Bus allocation / protocol selection**
- **Channel partitioning**
- **Protocol, transducer insertion**
- **Inlining**



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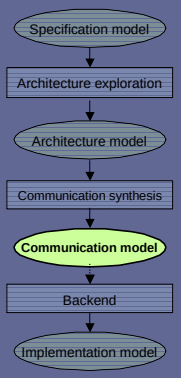
Communication Model

- **Component & bus structure/architecture**
  - Top level of hierarchy
- **Bus-functional component models**
  - Timing-accurate bus protocols
  - Behavioral component description
- **Timed**
  - Estimated component delays



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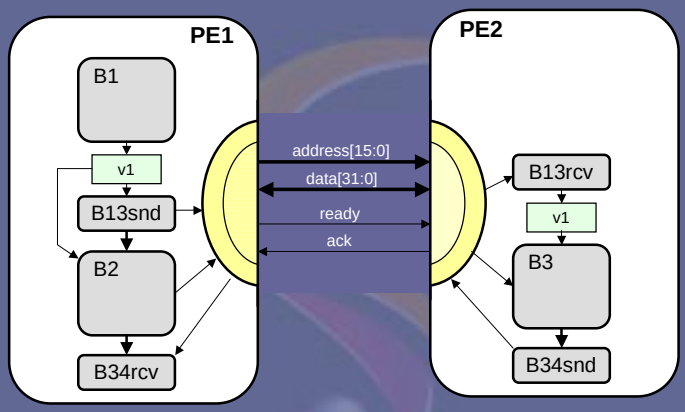
Communication Model Example



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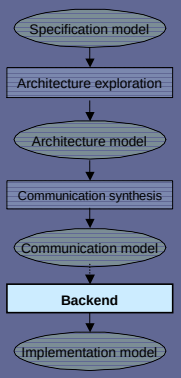
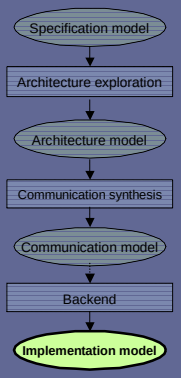
Backend

- **Clock-accurate implementation of PEs**
  - Hardware synthesis
  - Software development
  - Interface synthesis

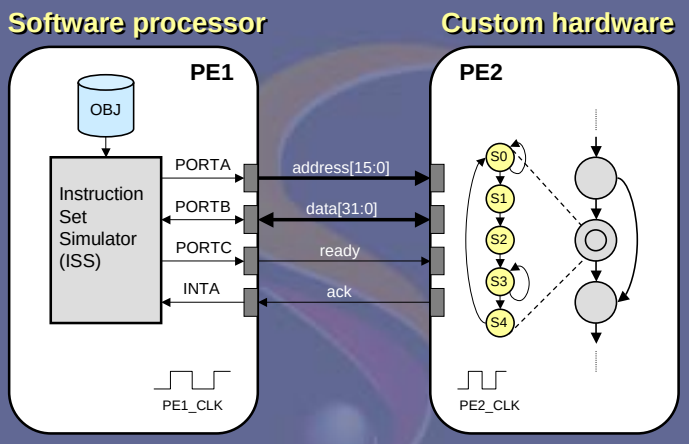


Implementation Model

- **Cycle-accurate system description**
  - RTL description of hardware
    - Behavioral/structural FSMD view
  - Object code for processors
    - Instruction-set co-simulation
  - Clocked bus communication
    - Bus interface timing based on PE clock



Implementation Model Example



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Summary and Conclusions

- **SpecC system-level design methodology**
  - Specification to RTL
    - System synthesis
    - Backend
  - Four levels of abstraction
    - Specification model: untimed, functional
    - Architecture model: estimated, structural
    - Communication model: timed, bus-functional
    - Implementation model: cycle-accurate, RTL/IS
  - Well-defined, formal models & transformations
    - Automatic, gradual refinement
    - Executable models, testbench re-use
    - Simple verification
  - Customizable
    - Easy integration with existing design flow

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Further Information

- **Literature**
  - "*SpecC: Specification Language and Methodology*" by Gajski, Zhu, Dömer, Gerstlauer, Zhao, Kluwer Academic Publishers, 2000.
  - "*System Design: A Practical Guide with SpecC*" by Gerstlauer, Dömer, Peng, Gajski, Kluwer Academic Publishers, 2001.
  - "*System-level Modeling and Design with the SpecC Language*", Ph.D. Thesis R. Dömer, University of Dortmund, 2000.
- **Online**
  - SpecC web pages at UCI **`http://www.cecs.uci.edu/~specc/`**
  - SpecC Open Technology Consortium (STOC) **`http://www.specc.org/`**

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Backup Slides

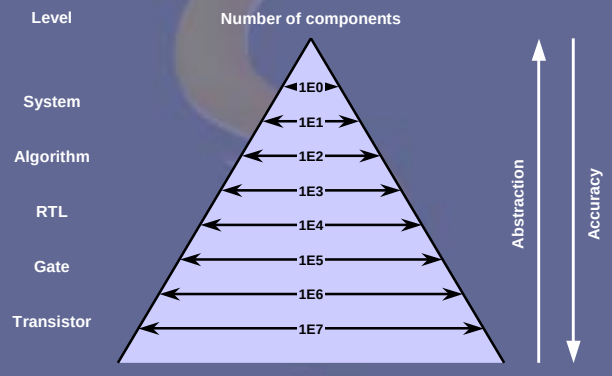
SpecC Technology Open Consortium

- Abstraction Levels
- SpecC Model
- Plug-and-Play

Introduction

SpecC Technology Open Consortium

- System-on-Chip (SOC) design
- Increase of design complexity



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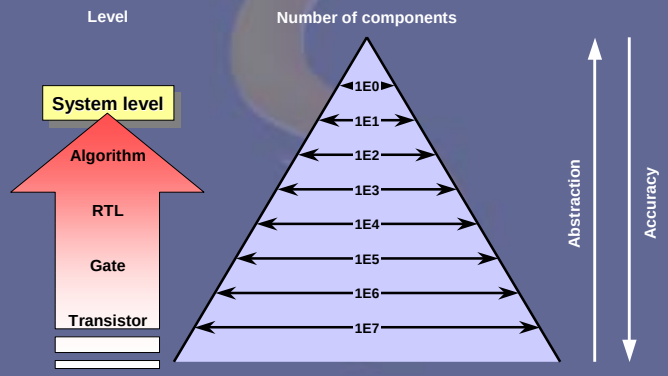
Introduction

- System-on-Chip (SOC) design
- Increase of design complexity
- Move to higher levels of abstraction



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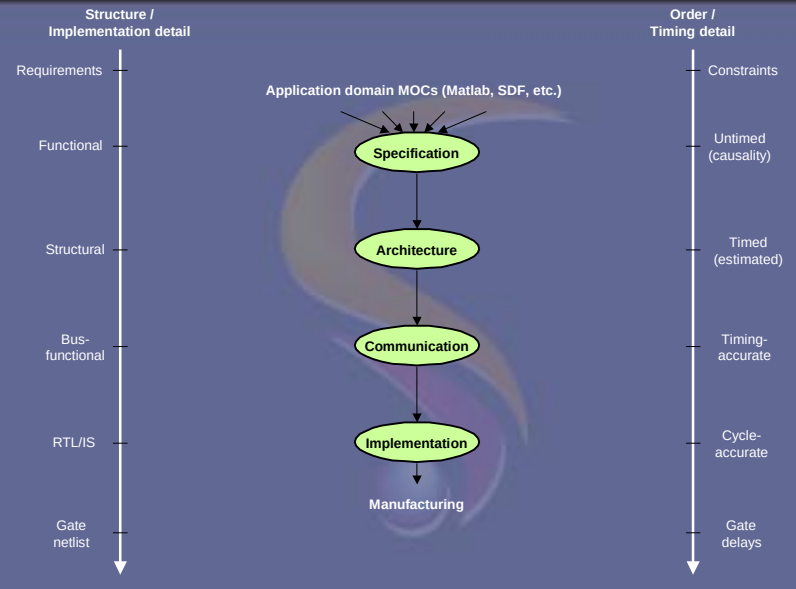
Abstraction Levels



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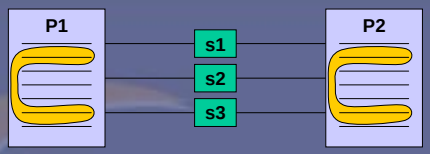
The SpecC Model

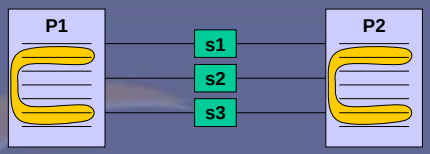
- **Traditional model**



  - Processes and signals
  - Mixture of computation and communication
  - Automatic replacement impossible

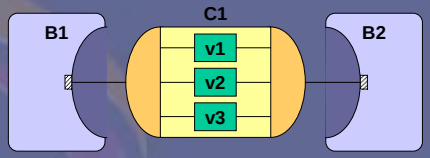
The SpecC Model

- **Traditional model**



  - Processes and signals
  - Mixture of computation and communication
  - Automatic replacement impossible

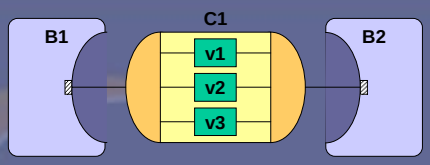
- **SpecC model**



  - Behaviors and channels
  - Separation of computation and communication
  - Plug-and-play

The SpecC Model: Protocol Inlining

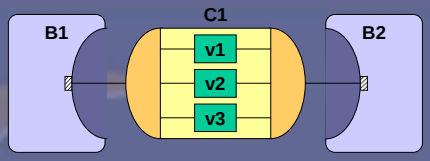
- **Specification model**
- **Exploration model**



  - Computation in behaviors
  - Communication in channels

The SpecC Model: Protocol Inlining

- **Specification model**
- **Exploration model**



  - Computation in behaviors
  - Communication in channels

- **Implementation model**

  - Channel disappears
  - Communication inlined into behaviors
  - Wires exposed

The SpecC Model: Plug-and-Play

- **Computation IP: Wrapper model**

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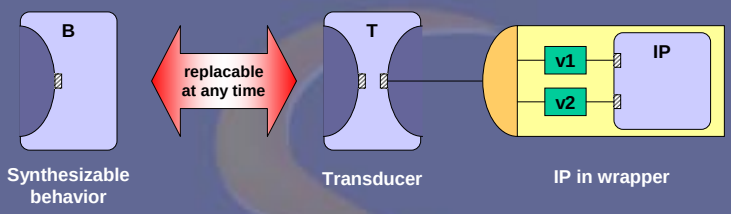
The SpecC Model: Plug-and-Play

- **Computation IP: Wrapper model**



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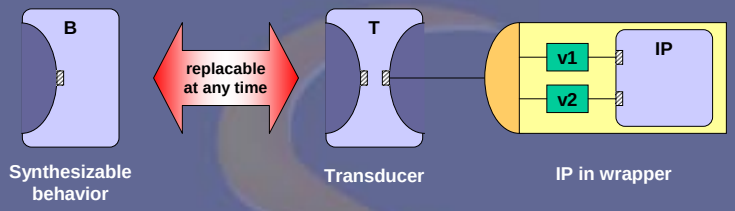
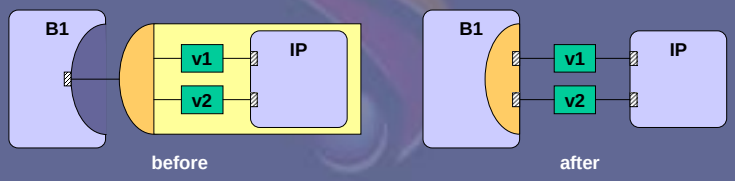
The SpecC Model: Plug-and-Play

- **Computation IP: Wrapper model**



- **Protocol inlining with wrapper**



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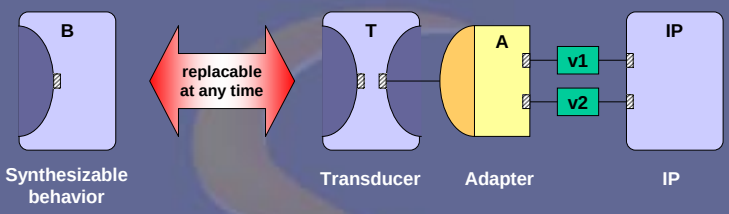
The SpecC Model: Plug-and-Play

- **Computation IP: Adapter model**



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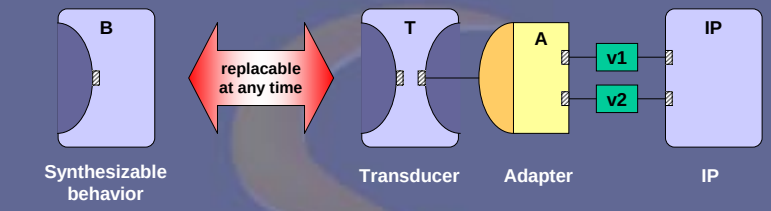
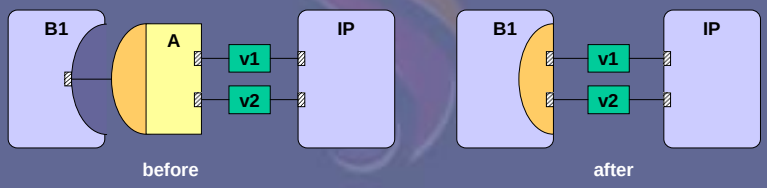
The SpecC Model: Plug-and-Play

- **Computation IP: Adapter model**



- **Protocol inlining with adapter**



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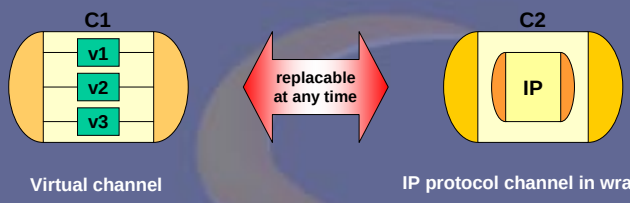
The SpecC Model: Plug-and-Play

- **Communication IP: Channel with wrapper**



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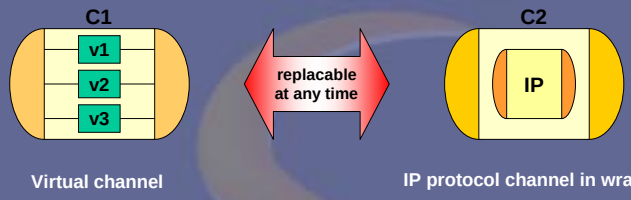
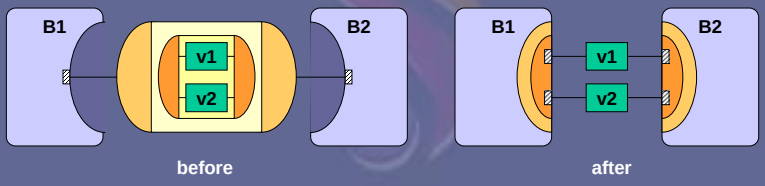
The SpecC Model: Plug-and-Play

- **Communication IP: Channel with wrapper**



- **Protocol inlining with hierarchical channel**



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Summary

- **SpecC model**
  - PSM model of computation
  - Separation of communication and computation
  - Hierarchical network of behaviors and channels
  - Plug-and-play
- **SpecC language**
  - True superset of ANSI-C
    - ANSI-C plus extensions for HW-design
  - Support of all concepts needed in system design
    - Structural and behavioral hierarchy
    - Concurrency
    - State transitions
    - Communication
    - Synchronization
    - Exception handling
    - Timing

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Conclusion

- **SpecC language**
  - Executable and synthesizable
  - Precise coverage of system language requirements
  - Orthogonal constructs for orthogonal concepts
- **Impact**
  - Adoption of SpecC in industry and academia
  - SpecC Open Technology Consortium (STOC)
- **Future**
  - Standardization effort in progress by STOC
  - Improvement with your participation

Conclusion

- **Using the SpecC language and the advanced architecture exploration capabilities of the SpecC methodology, architecture exploration is quick and easy to implement in the abstract level.**
- **Reuse can be done from the component level to the system level.**
- **Productivity gain from working at higher levels of abstraction.**