Semicustom Design: Synergies Between Full Custom and ASIC Design Flows in High-Performance Processor Design

Greg Northrop
IBM Research
Yorktown Heights, NY

Abstract

The quest for performance through high frequency in the design of micro-processors has lead a number of approaches, including deep pipelining, and the use of aggressive (dynamic) circuit styles. However these designs, particularly ones implementing complex architectures, still have a heavy reliance upon more conventional static CMOS design styles, particularly for control logic. Combined with the fact that supply voltages are not fully scaling, leading to increased power densities, it is likely that static CMOS will play either a fixed or increasingly important role in high performance design. Given the numerous pressures on the design process, primarily the concurrent closure on cycle time, circuit and physical design, and functional verification, and the need for reliability and testability during hardware bringup, there has been a strong need to optimize static design in both performance and "time to market".

This paper describes techniques used to improve cycle time performance in both synthesized and custom circuit design in the context of the development of the last couple of generations of the central processor used in the IBM zSeries (formerly S/390) mainframes. These processors implement the complete S/390 architecture (over 1000 op-codes) in a single chip, the latest in 0.18u technology with a clock frequency of over 1GHz. The circuit style is predominantly static (outside of the SRAM), implemented using both custom design and a heavily customized synthesis and standard cell methodology.

A parameterized representation of simple static gates (inverters, nands, nors, etc) is used as the starting point for both synthesis and a semi-custom design flow. The synthesis flow includes a custom "tall thin" library, gain-based synthesis, and numerous other optimizations to achieve maximum performance in control logic. The "tall thin" library contains predominantly the simple single-level inverting CMOS types, but in a large number of variants and sizes. This dense set of primitives gives synthesis the greatest range of options to achieve performance. The semi-custom flow leverages both the cell generation technology used to implement the synthesis library and the place and environment developed for synthesized logic, and adds circuit tuning (sizing) tools to achieve improved performance and greatly increased turn-around-time in important and performance sensitive types of combinational function.