Open Physical Design Rule initiative and Open Design Rule Description Language.

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Abstract
In this paper we present an open physical design rule description language for DSM ASIC
development. This work is a complement effort to the Open Physical Design Rule (OPDR)
initiative which has been promoted by STARC*. OPDR is a set of physical design rules such as mask design rule and Spice parameters with real numbers on each rule. Once it in place, many OPDR adopting semiconductor manufacturers will offer their processes which support OPDR. There are many exciting things come out with this. For example IP and SoC designs will be far more portable among these manufactures.
STRAC unveiled preliminary OPDR for 130nm CMOS SoC process as of September 2000.
During the development of OPDR, they discovered a serious problem on lacking a standard for physical design rule interchange between groups such as process engineers
and circuit designers. Now we urge necessity of the unified open physical design rule description language (OPDRDL) and propose our preliminary specification for it.
Also we present early version of a tool for the execution of the OPDRDL.

*STARC: Semiconductor Technology Academic Research Center, Japan (www.STARC.or.jp)

1. The big picture: Industry Open Physical Design Rule.

The semiconductor industry has been challenged by new paradigm change in both technology and business. The deep sub-micron (DSM) process technology makes several traditional system level functions available together on a single small chip. More the process becomes delicate, more it depends on manufacturing equipment. Cost of one DSM wafer factory will sore to more than three billion dollars. These are a few of many reasons why the industries jointly organize ITRM (International Technology Road Map) committee to assess future direction of semiconductor technologies.
With all these indicators, industries will have to be very serious about their business models such as scale merit of mass production, risk hedge, focused engineering resources. Even top group semiconductor manufactures trouble to have the luxury to afford all necessary expenditure to build and run next generation wafer factory by themselves. This is the reason why we have heard of so many semiconductor alliances among the world.

There are many reasons for the palladium change in the design side also.
Although functionality of these chips is endlessly bigger and more complex, the life of these chips become shorter and shorter. Also design cost of these chips become very expensive. New expensive factories are so hungry for immediate products. There are lots of reasons why industry have to consider new technology and business paradigm.
Following this story to the extreme. There is a scenario where industry selects one de-facto standard process. Then every company manufactures their chips by the process. Beside, IP providers design various IPs by the design rule based on the de-facto standard process.
System manufacturers and design houses build system-on-chips on these IPs.

Real business world might not be so simple as the scenario above. Instead of such revolutionary change, we can consider more evolutional paradigm shift. One possible

scenario is to standardize on design rule rather than standardize process itself. Some one called this scenario as the new meet-in-the-middle concept**. Both design and process people meet in the Open Physical Design Rule.
Other words, both groups of process and circuit designers share same open mask design rules and Spice parameters together as their committed physical design rule. Wafer foundries can keep their freedom to choose their own process. Design side can accumulate IPs, which are reusable and portable among these manufacturers that commit to the open design rule. We call this open physical (actually with electrical) design rule as OPDR.

STRAC has initiated the Open Physical Design Rule project (Code name: Namazu/Catfish).
Researchers in STARC explore technical feasibility of the Open Physical Design Rule based SoC development. Also the researchers will investigate some aspect of the business model for the OPDR deployment among industry and academia. As of September 2000 STARC disclosed outline of their 0.13u OPDR to the public. Now they are working on detailed design of it.

**Meet-in-the-middle: Professor Hugo deMan, K.U.Luven used this word first for his hierarchical design methodology.

2. Open Physical design rule description language: Necessary and is an important vehicle.

Once the OPDR is accepted, there are lots of paradigm shifts that will follow.
With OPDR, it is possible to share and exchange various ready-to-use information among the industry and academia. To fulfill this opportunity fully, we need the Open Design Rule Description Language (OPDRDL). With OPDRDL process developers, IP providers and system chip designers share mutually necessary information to take full advantage of OPDR.
There are many new opportunities can be arise. For example process developer can analyze and tune their process technologies to minimize deviations, maximize yield.
IP provider can research new circuit, logic and architectures with stable and real design rules in hand. Among all, system chip designers can design their SoC efficiently with handful proven IPs supplied by multiple IP providers. We very much welcome university involvement in all of these activities. These researchers can access open standard design rule for the specific process generation written in OPDRDL. It should be open to public and be shared among them.
There are several key conditions that have to be satisfied as for OPDRDL:
-It must have strong descriptive capability to handle all necessary rules required by OPDR.
-It must handle not only OPDR but also include manufacturer proprietary physical design rules (PPDR).
-It must be readable, clear and versatile so that designers with various backgrounds can use the language as a tool for communication.
-It must have open and expandable architecture by which process, IP and SoC designers can tune it for their demand.
-It must have a capability to handle complex ownership of mixed open and private physical design rules.
-Affordability for everybody.

3. Current status of the physical design rule description language.

The OPDR is not a popular concept yet in the semiconductor industries, so as OPDRDL.
Following are very common observations among semiconductor industry.
When process developers and design engineers come together to discuss their design rule, most common tools are pen and paper, even not laptops.

This tells us here there is bottleneck overcome to build smooth electrical data flow between design and manufacturing communities. Most of current design rule languages are merely input for a specific EDA tools such as DRC and auto router. Therefore these languages don't have most of the capabilities listed above on a requirements list.

<< Example of Dracula or Caliber DRC Language >>

However there are several excellent activities and products available.
FSA (Fabless Semiconductor Associate (www.fsa.org) Physical Design Rule Format Standard (PDFS). DSM Technologies (www.dsmtech.com) GTE / FLG tool set.
PDRF has several nice features because of its original purpose, use for exchange design rules among industry. These features include

- Open to public as free.
- Clean and readable textual language.
- Rules and values are separately managed.

However there are several unsatisfied issues for our use model.

- It does not support basic shape level operations such as AND, OR, XOR directly.
- Too many process dependent design rules. Lack of meta-language for shape manipulation (same as above.)
- No graphical language support.
- Lack of the capability to support private rules.
- Only the language, no existing tool support.

METAL □

Rule	Unit	Min/Max/Exact	Description
601	um	min	m1 width
602	um	max	mi width
603	um	exact	
604	um2	min	m1 area
605	um2	max	m1 area
606	um	min	m1 enclosed area
607	um	min	m1 space to m1
608	um	min	m1 notch width

□□□**<< Example: FSA PDRFS description >>**

Design rule editor from DSM Technologies Inc. has unique and nice feature set such as

- Excellent graphic interface.
- Strong ability to handle complex shapes and rules.

However this tool also has different use model.

- Proprietary language.
- Mixing rules and their values as a set.
- Lacks capacity to manage complex ownership of rules.
- No API support. Only has straight output for DRC etc.
- Expensive.

During the development of OPDR we discovered a serious problem on lacking a standard for physical design rule interchange between groups such as process engineers and circuit designers. Based on these situations, STARC has initiated an Open Physical Design Rule Description Language project (Code name: Bazaar), which will complement Namazu deployment in large SoC community.

3. Open Physical Design Rule Description Language (Bazaar).

Followings are the outline of basic requirements, specification and current development status of Bazaar.

3.1 Requirements.

Objective of Bazaar is to provide consistent foundation for the open design rule based chip design (Namazu). Bazaar must satisfy the following requirements

- Heterogeneous but unified design rule description language that capable to describe all Namazu requirements.
- Strong data management capability that is required to manage public and private data together in unified framework.
- Must provide execution environment (tool).
- Strong GUI and network ready capabilities that support instantaneous, interactive communication among designers and tools.
- API which links design rule to other chip design tools such as DRC, Cell generator, Auto layout, T-CAD, yield estimator and so on.

3.2 Specification.

Bazaar requirements are consists of two-parts (1) Specification of Bazaar language, (2) Specification of Bazaar execution environment (tool).

3.2.1 Specification of Bazaar language.

3.2.1.1 Mixed textual and graphical language.

Text: Structure of data hierarchy, data ownership, Mathematical operation, Electrical parameter.

Graphical: Online shape edit, online rule data input and checking, 2D/3D, electrical simulator I/O.

3.2.1.2 Functionality of Bazaar language

1.2.1 Public vs. Private: This allows manufacturers separate their private design rule from open design rule.

1.2.2 Three step rule definition.

1. Basic mathematical operators.
2. Actual rule set without values.
3. Actual value set for each design rule.

1.2.3 Capable to define process induced rules and design-induced rules separately. Typical design induced rules are special angled lines, limited shape of contacts.

1.2.4 Co-existence of multiple process induced rules.

Logic block, DRAM block, Low voltage block, I/O block and so on.

Assumption these blocks use their unique process.

1.2.5 Capability to manage the ownership of each rule.

3.2.2 Specification of Bazaar environment.

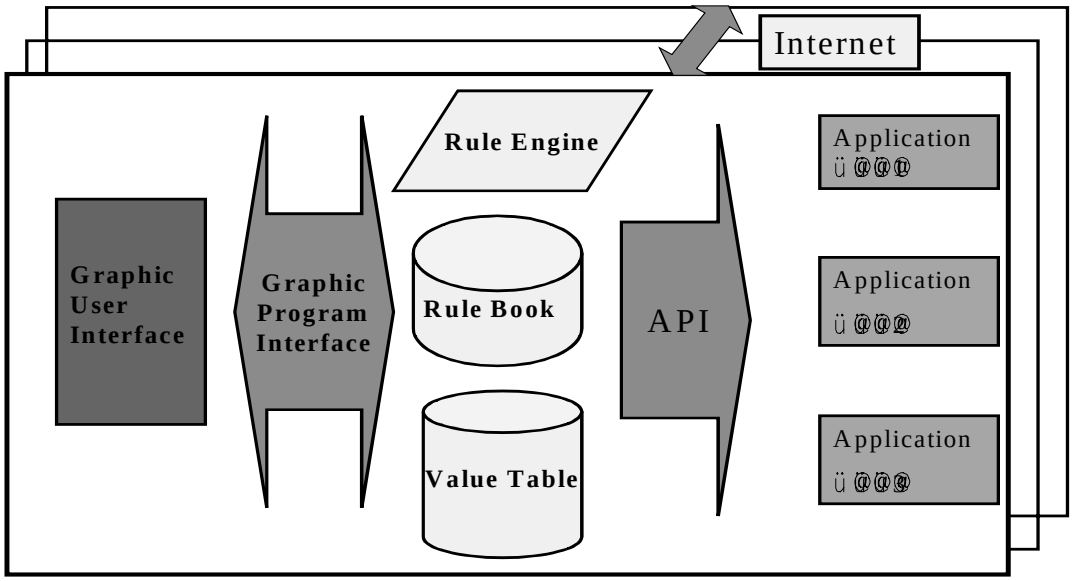
3.2.2.1 Open and flexible architecture for future expansion and customization.

3.2.2.2 Network ready capability to support distributed heterogeneous design community.

3.2.2.3 Clean and open API enable to link design rules to related EDA tools.

3.2.2.4 Hardware platform free.

3.2.2.5 Source code availability for the industry-and-academia-wide discussion and enhancements.



Bazaar Architecture

3.3 Bazaar Grammar outline.

3.3.1 Basic structure.

- Hierarchical language with XML like structure with reserved words.
- Examples of Reserved words.

< Owner > Name < /Owner >
< Public > Name < /Public >
< Private > Name < /Private >
< Rule-by-Process > Name < /Rule-by-Process >
< Rule-by-Design > Name < /Rule-by-Design >
< Rule > Name < /Rule>

3.3.2 Design rule description.

Currently we are examining FSA PDRFS (Physical Design Format Standards) as our starting material. PDRFS is an open standard format, which has been developed by FSA. Different from others, it is defined to be a standard for design rule exchange among industries. PDRFS has been opened to everyone.

Currently FDRFS has over 900 rule descriptions for 0.25u CMOS process. Also it has large taxonomy and library, which are very valuable to share. However we found there are several open subjects to be developed. Some of these are graphical languages, hierarchical ownership management, mixed design rules. Also we need to develop API for application tool linkage.

3.4 Bazaar execution environment (Bazaar tool)

We strongly believe Bazaar should be open to the community with its execution environment (Bazaar tool). From its requirement, the tool will be based on JAVA / XML, platform-free and network-ready architecture. Bazaar tool should be very easy to use and expandable in everywhere including university classrooms.

These are many this and that have to be checked up. Some of these are the distributed database management and real time graphic base communication among long distance engineers. These matters will eventually be solved with explosively dynamic Internet technology development.

3.5 Bazaar milestone.

Namazu has immediate needs of Bazaar. Currently it has been using legacy P&P tool to define 0.13u OPDR. At the same time we are examining PDRFS capability for Namazu design rule description.

As of EDP-2001 workshop, we plan to present straw man proposal for Bazaar language structure, grammar and semantics. Also we are going to demonstrate mock-up of Bazaar GUI. First official specification of Bazaar and working prototype will be available on late 2001.

4.Summary.

STARC has been working on their open physical design rule project (Namazu: Catfish) for 130nm CMOS SoC process. Currently they have to use legacy pen & paper approach. But sooner or later they must have powerful environment to support industrial use of Namazu. Bazaar is the complementary project with Namazu to provide the infrastructure where Namazu swim. If Namazu survive and grow to be a whale so does Bazaar.

With this ambition, we would like to open Bazaar for discussion with anyone who is interested.