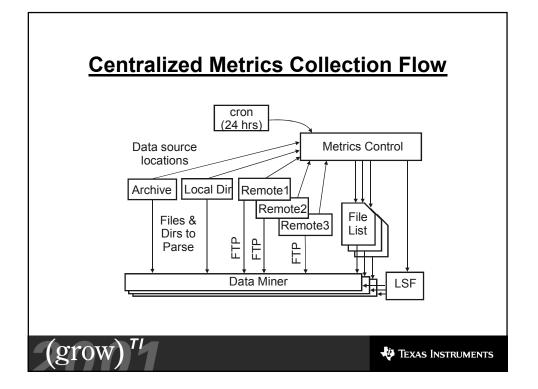


Metrics Collection Programs

- Metrics Control Program
 - Determines all the possible files and directories that need to be analyzed
 - Creates many file/dirs lists that get submitted to data mining program (via LSF) to be analyzed
- Data Mining
 - Determines if a file/dir has changed (via the timestamp) since last time and, if so, parses the file again and adds/updates the Oracle database

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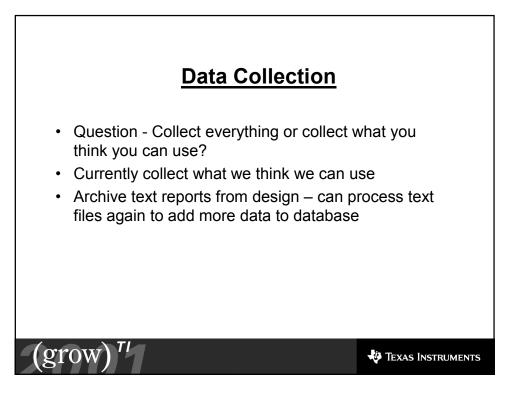


Oracle Metrics Tables

- Designs Table List of designs
- Details Table Lists of design attributes
- Steps Table List of steps executed in flow
- Macros Table List of macros (cells, I/Os, macros, and subchips) used in the design
- MacroSize List of sizes of macros
- File_Stats Last timestamp of listing file



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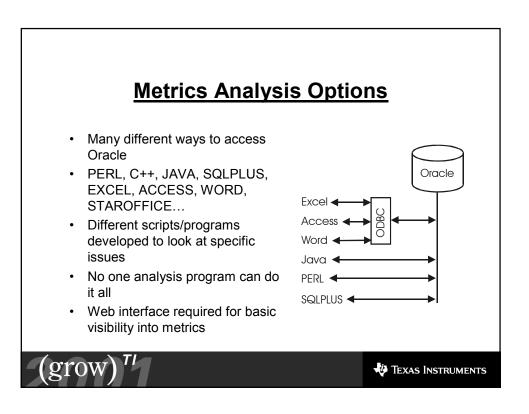


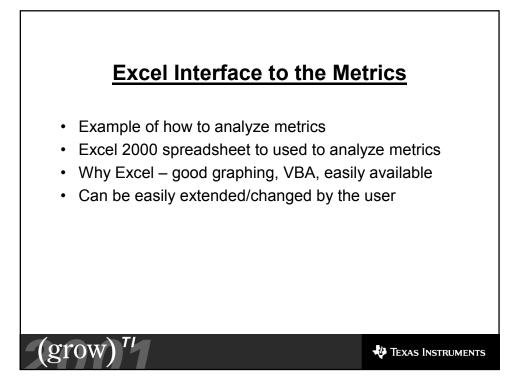
Metrics Collection Issues

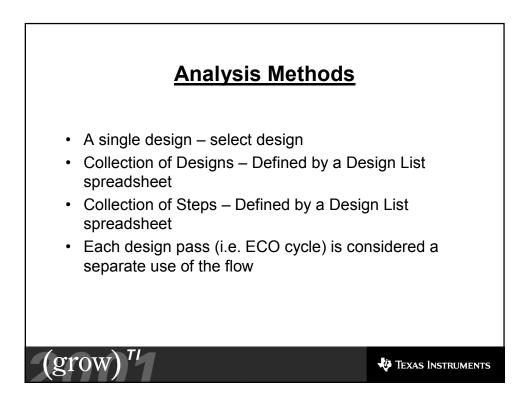
- The physical design process was not designed with metrics collection in mind
- · Not all data available that you would like to have
- Missing designs since there is not 100% coverage from the collection process
- Some data about a design is missing since there is no checking to make sure it exists
- Common way to collect/save data when several different layout tools are used (Apollo, Astro, Magma, PC)

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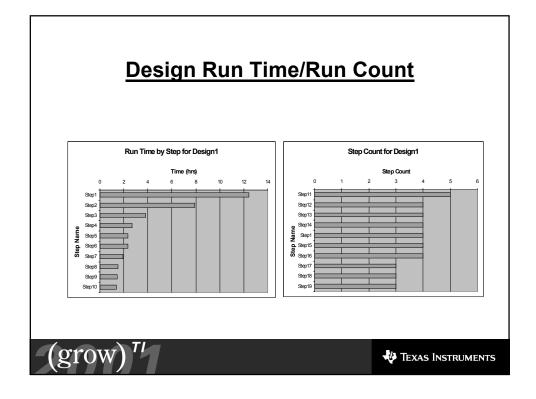


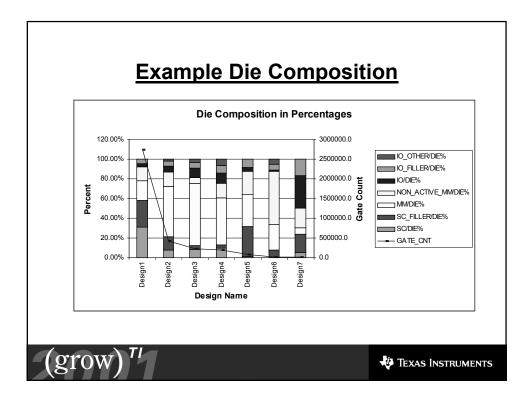


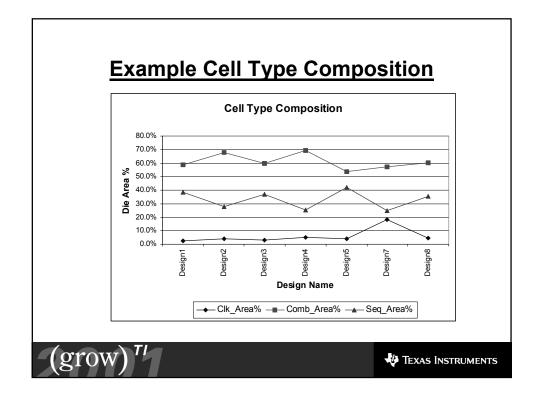


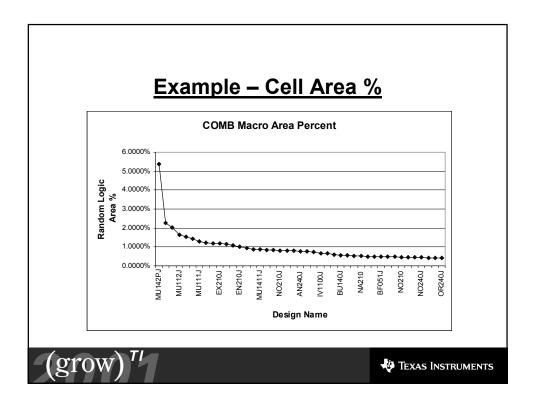
Pass 2/5/01 1:52/04 AM Timeline Spre Wildth of Plot (in columns) Desi 10 Step Plot Timeline Stu Plot w/Rework Step Output Workbook edps.xls	Design Design 1	xustom	
Hide	_		

-	A	B	C	D	E	F	G
1	Step-Tot Days= 8.47 Step Name		-VVht space	(days) 6.45, Recy	cie time (days)= 1	.02	
2	Step Name Step1 (1)	0.319					
4	Step1 (1) Step2 (1)		1		1	1	
5	Step2 (1)						
6	Step4 (1)		I	1		I	
\$7	Step5 (1)	0.188	1	1	1	1	1
8	Step6 (1)	0.164	J				
9	Step7 (1)	0.018		- H			
10	Step8 (1)	0.001		Li .	I	i	i
	Step9 (5)	0.761			1 I	I (
	Step10 (4)	0.157					
	Step11 (4)	0.017			1		
	Step12 (4)	0.013		1		L	
	Step13 (4)	0.041		1.1		1	
	Step14 (3)	0.113		1 1		· · · ·	
	Step15 (3)	0.170				i	
	Step16 (3) Step17 (4)	0.301					
	Step17 (4) Step18 (2)	0.033					
	Step10 (2) Step19 (2)	0.003		1			
2	Step15 (2) Step20 (2)	0.001			1	1	







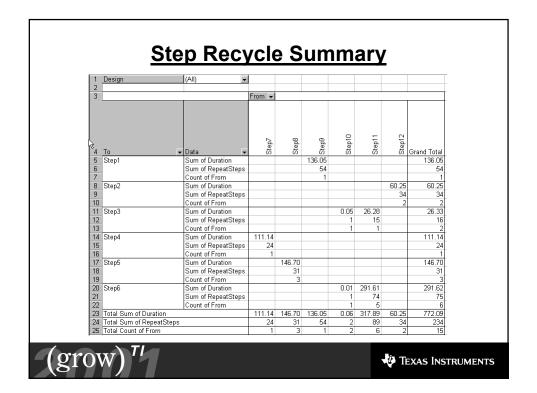


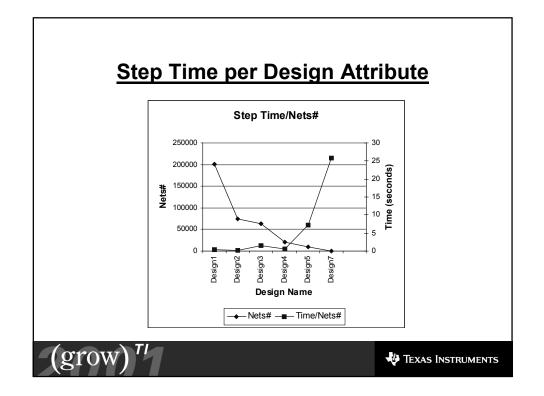
Runtime for Several Designs

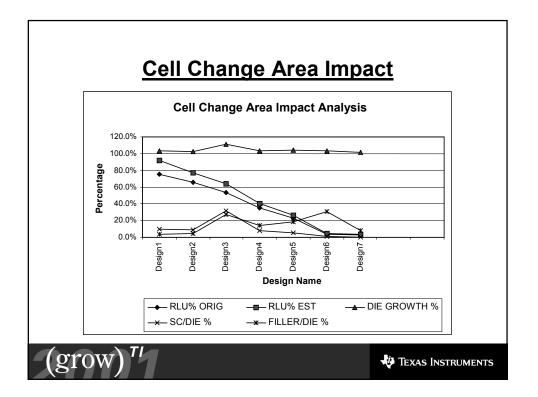
	A	В	С	D	E	F
1	StepName (Designs = 7)	TotalTime	TotStepCnt	MinTime	MaxTime	AvgTime/Run
2	Step1	125.1	12	0.011	83.399	10.424
3	Step2	100.5	10	0.042	44.227	10.048
4	Step3	82.8	10	0.217	23.073	8.280
5	Step4	73.2	29	0.001	16.276	2.524
þ 6	Step5	46.6	52	0.003	3.795	0.896
7	Step6	46.5	91	0.003	7.852	0.510
8	Step7	35.2	17	0.121	10.690	2.070
9	Step8	34.9	29	0.001	3.412	1.203
10	Step9	31.2	26	0.002	7.346	1.198
11	Step10	29.8	24	0.001	10.352	1.242
12	Step11	28.2	28	0.006	3.311	1.006
13	Step12	27.5	36	0.001	4.431	0.764
14	Step13	27.3	36	0.001	4.060	0.759
15	Step14	21.4	10	0.013	8.512	2.139



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Types of Cycle Time Improvements

- · Steps being run in the flow when no input data was changed
- Improved ordering for steps in the flow (reduce time when there are recycle loops)
- Checks being run too late in the flow. Difficult to make changes to fix problem
- Checks being run too early in the flow. Design is not solid enough so no action is being taken with the output
- · Too much layout database extraction/conversion time
- Opportunities for parallelism in the flow not exploited
- ASIC architecture causing S/W to be overly complex/slow
- Poor input data quality causing recycle loops
- Improved algorithms for handling larger data volumes

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