Effects of Physical Design & Logic Synthesis Integration on Design Methodology

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Objectives of presentation

- Describe why synthesis and placement must be integrated
  - Timing objectives and wirability must be achieved to close designs
  - Increasingly difficult due to dominant interconnect delay of advanced technologies
  - Difficulty translates to longer design schedules

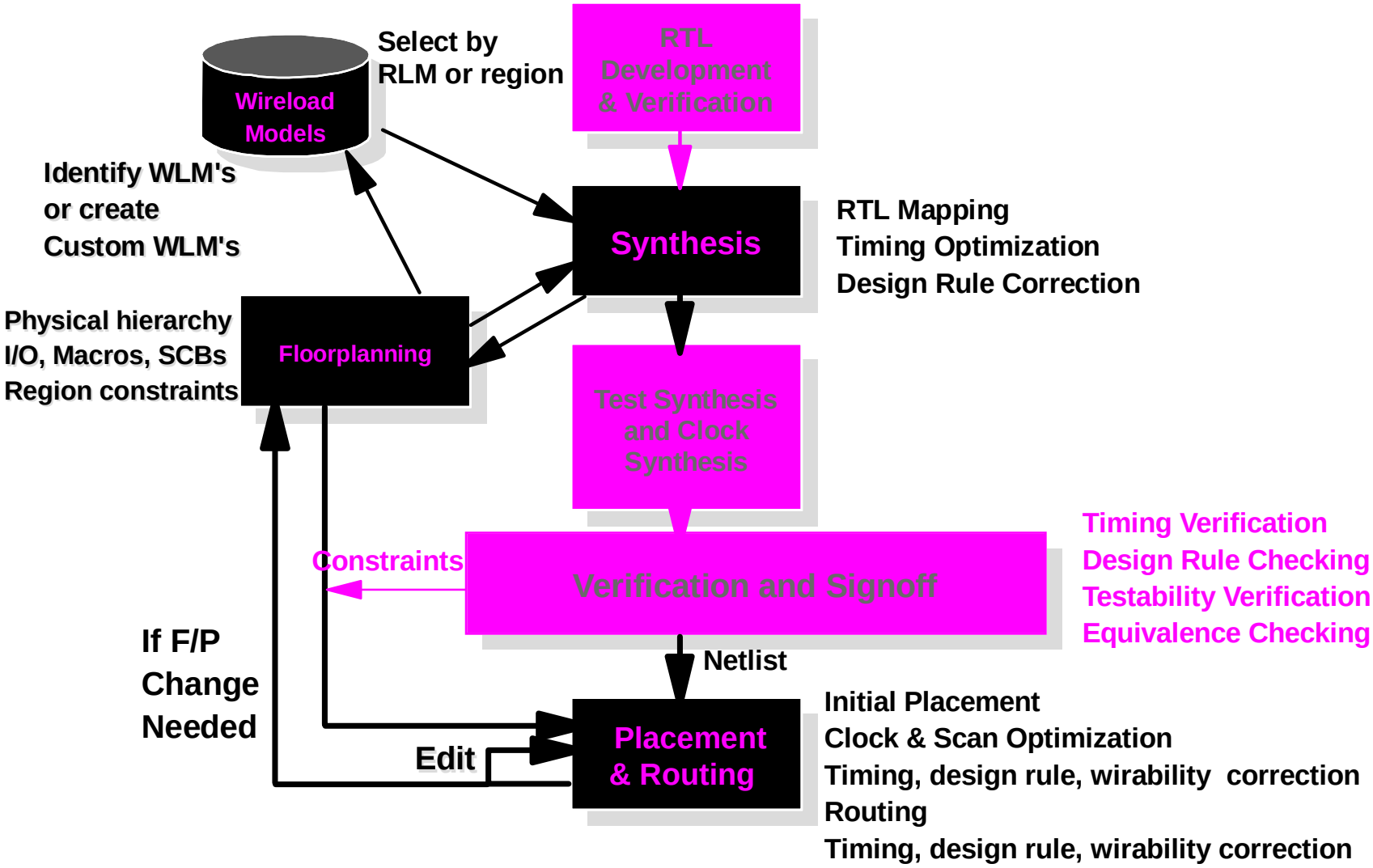
Objectives of presentation (cont.)

- Logic synthesis and placement can be integrated
  - Effectively attacks the schedule issues of timing and wirability closure
  - Can simplify aspects of design methodology
  - Tool interoperability improvements are needed

Overview of presentation

- Traditional Timing Closure methodology causes loops in the design flow & schedule
- Placement-based synthesis is proposed as a method of reducing the loops:
  a major step toward one-pass design
- Early timing closure and late timing closure applications
- Methodology integration
  - multi-vendor tool mix
- A view of total methodology integration

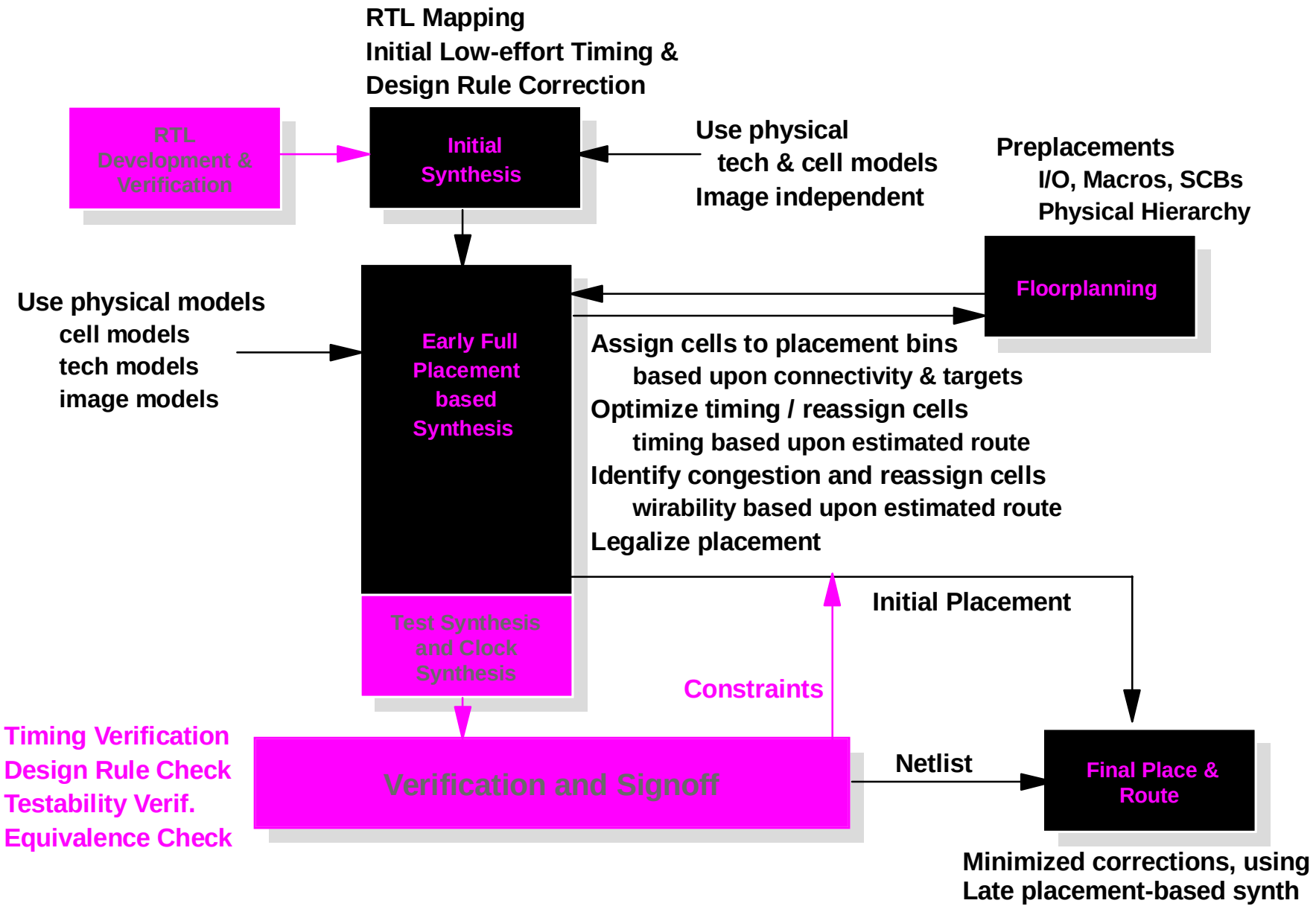
Timing Closure in today's Methodology Flow



Some problems with today's flow

- Loops in the methodology flow impact TAT
  - Front-end "inner loop:"
    Synthesis-Floorplanning-WLM
    - Complexity is aggravated by detailed WLM areas & regions
  - Backend "inner loop:"
    Timing, design rule, and wirability edits in layout
    - Poor correlation of WLM's to post-placement wiring causes late timing issues
  - "Outer Loop:"
    Re-floorplan and/or re-synthesis
    - Initial floorplan not wirable or can't close timing
    - A maior schedule killer

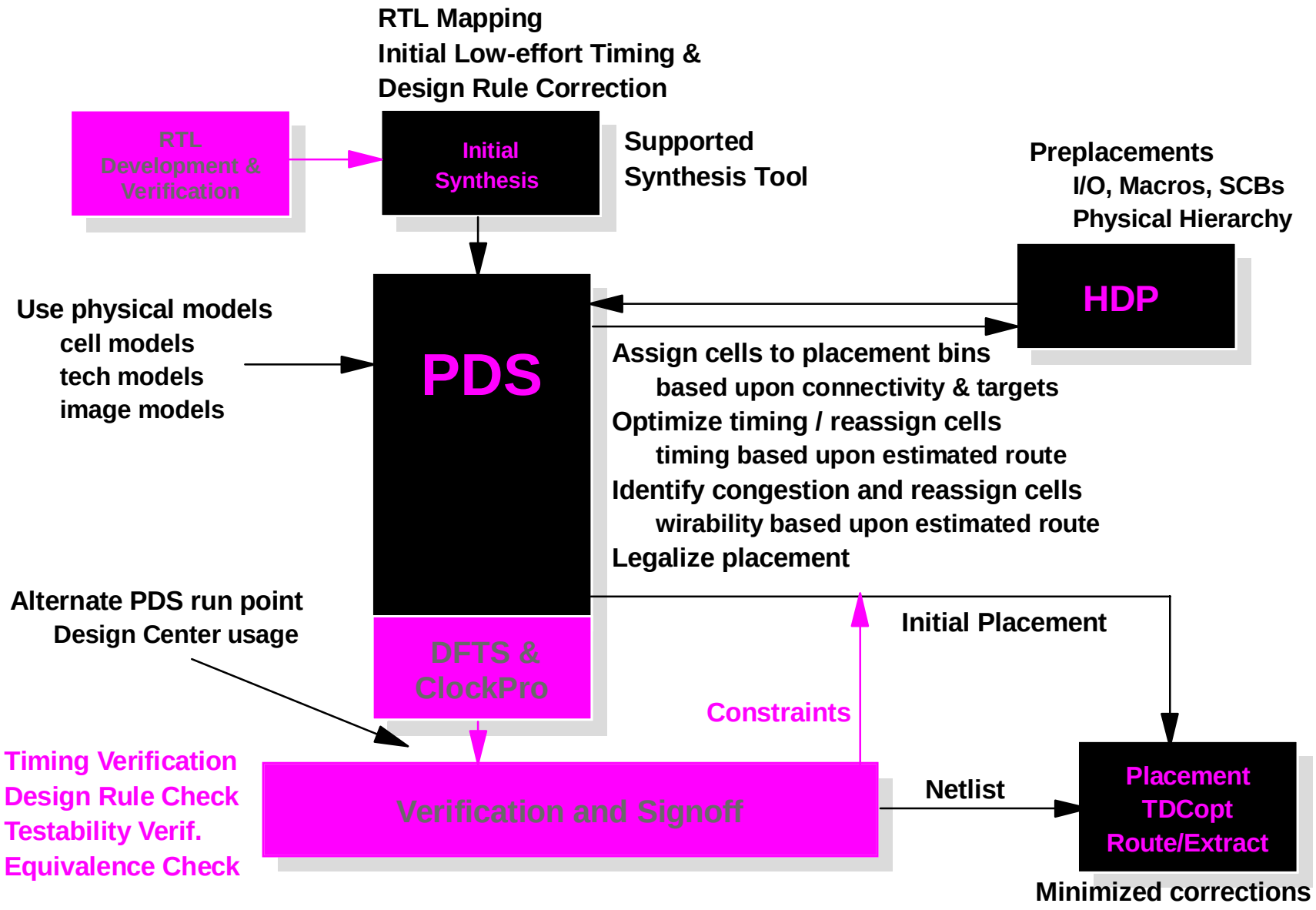
Improved Design Closure Flow



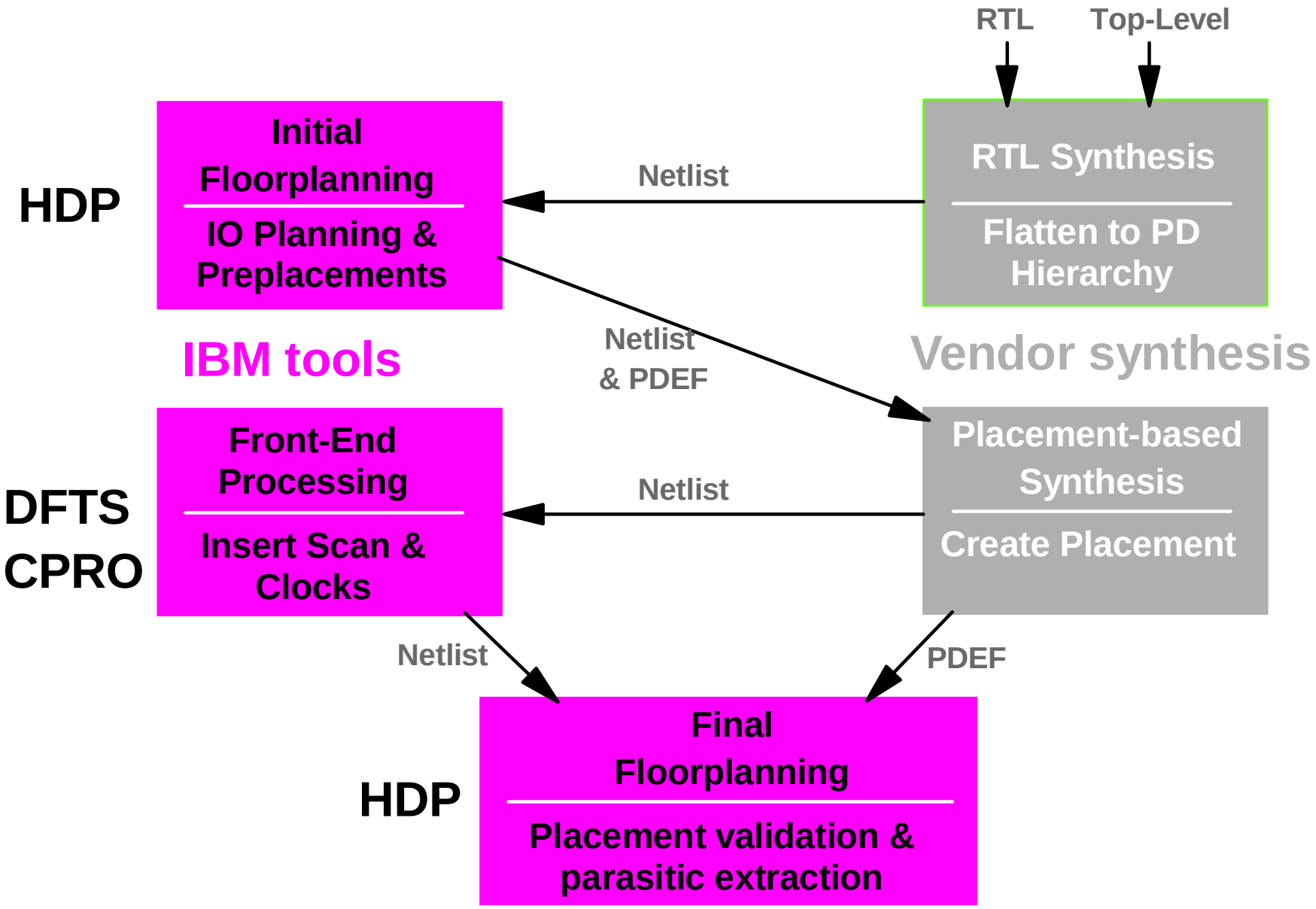
Affects on the methodology loops

- Front-end "inner loop:" *Synthesis-Floorplanning*
  - Detailed regioning for WLM choice not needed
  - Ability to drive placement eliminates WLM pessimism. Synthesis attacks the real problems.
- Backend "inner loop:"
  Timing, design rule, and wirability edits in layout
  - Correlation improved, reducing timing issues
  - Late synthesis-based correction methods reduce TAT for post-placement timing fixes
- "Outer Loop:" *Re-floorplan and/or re-synthesis*
  - Better timing correlation and more viable wirability minimizes bad initial placements

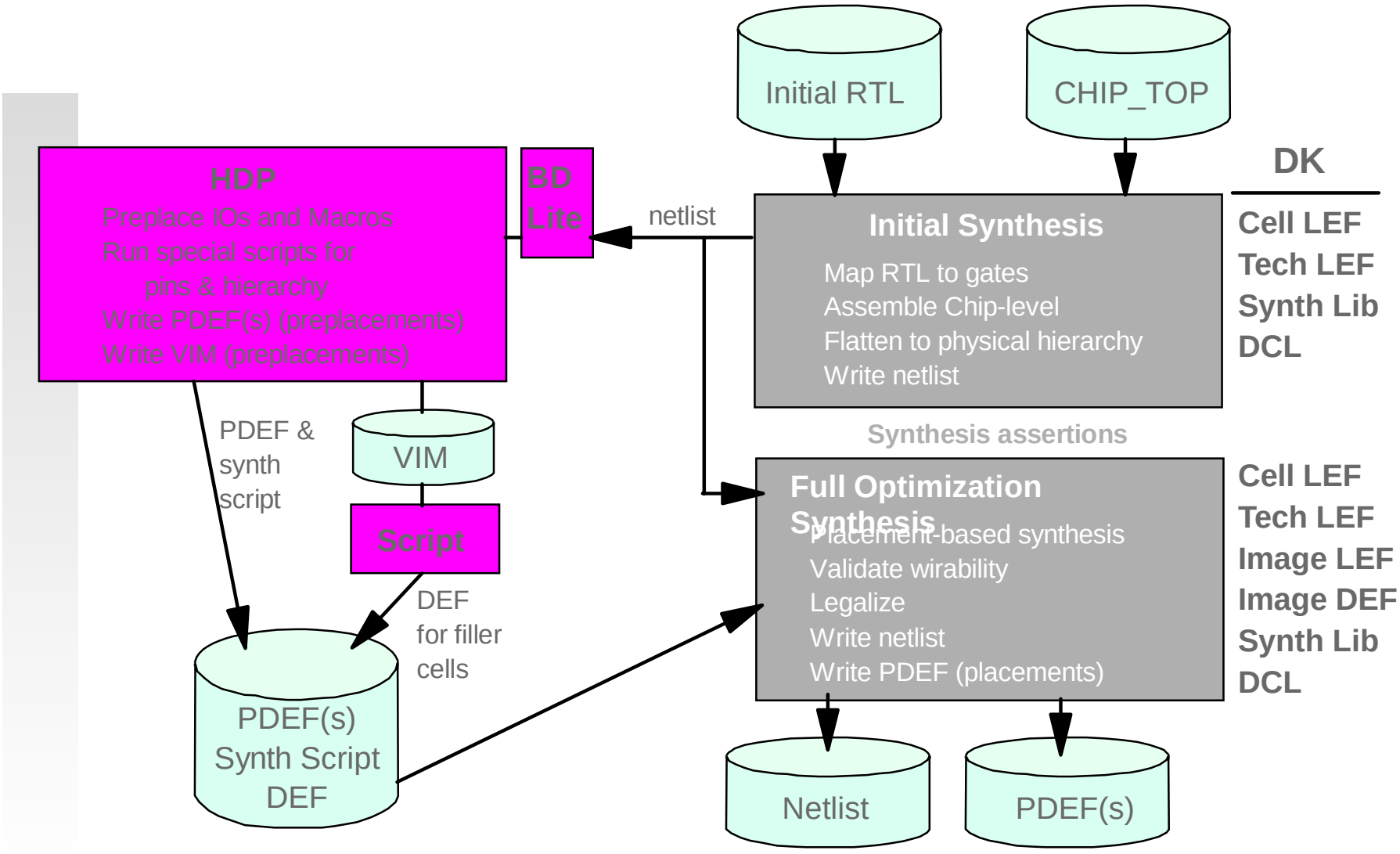
IBM PDS Full-Placement synthesis methodology



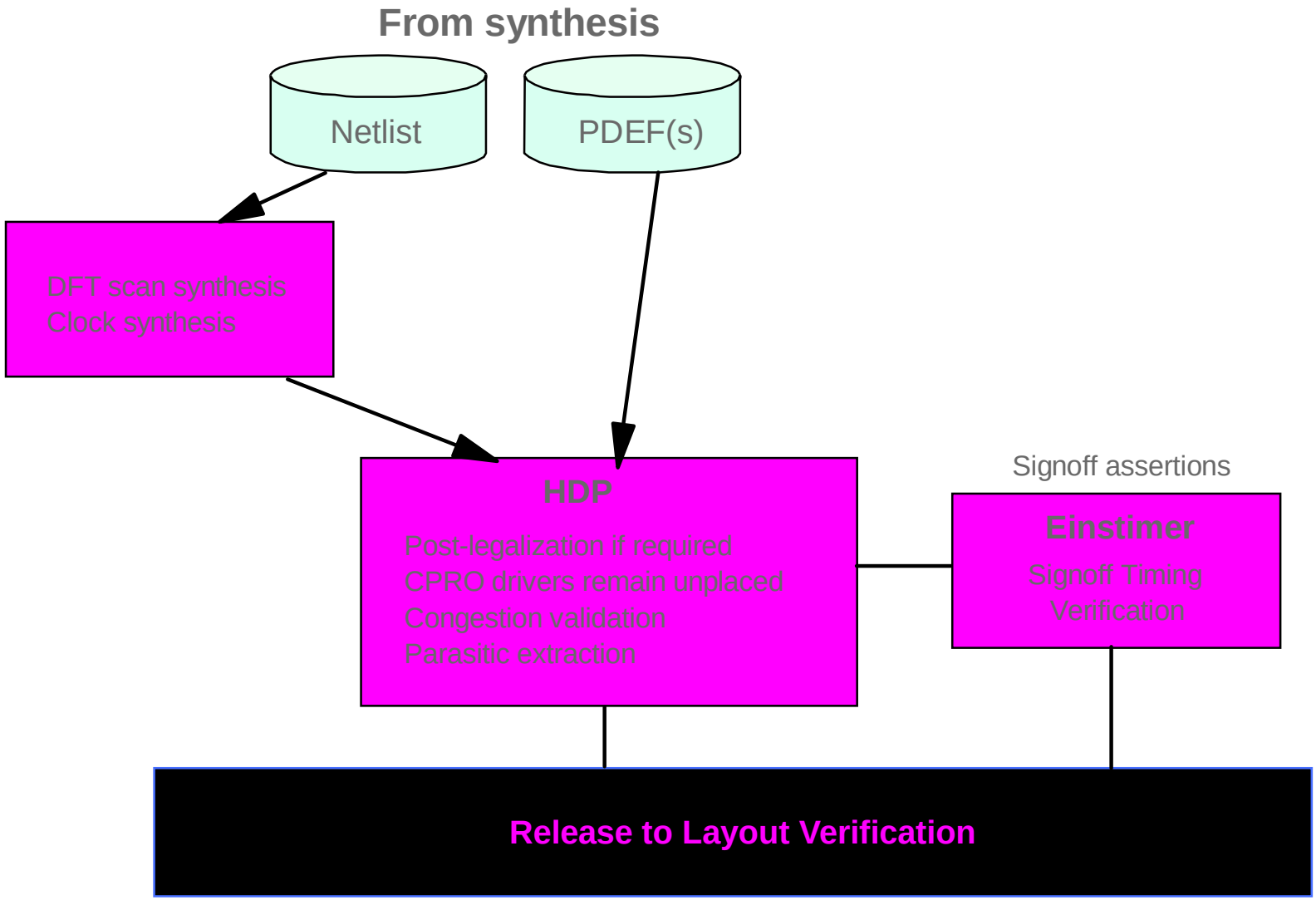
Multi-vendor Early Synthesis Flow



Early Synthesis and Floorplanning

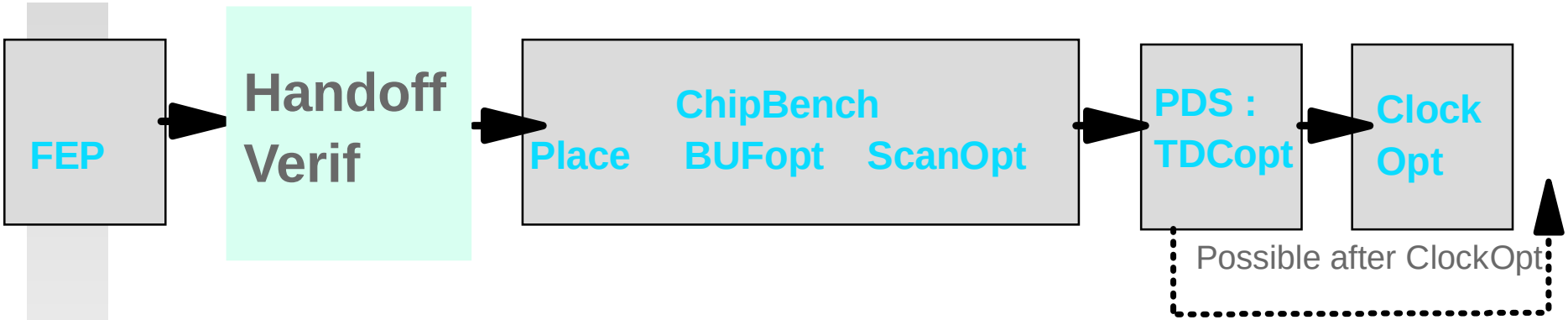


Post-synthesis thru signoff

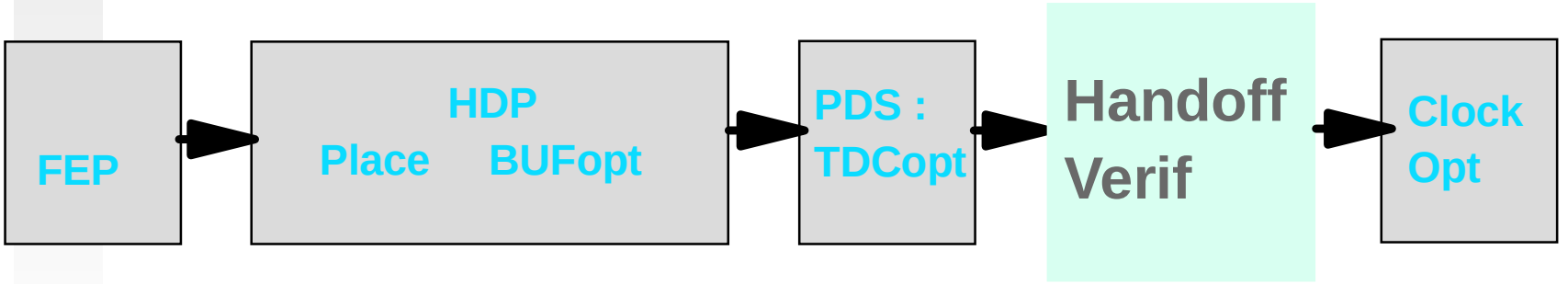


Late timing correction models

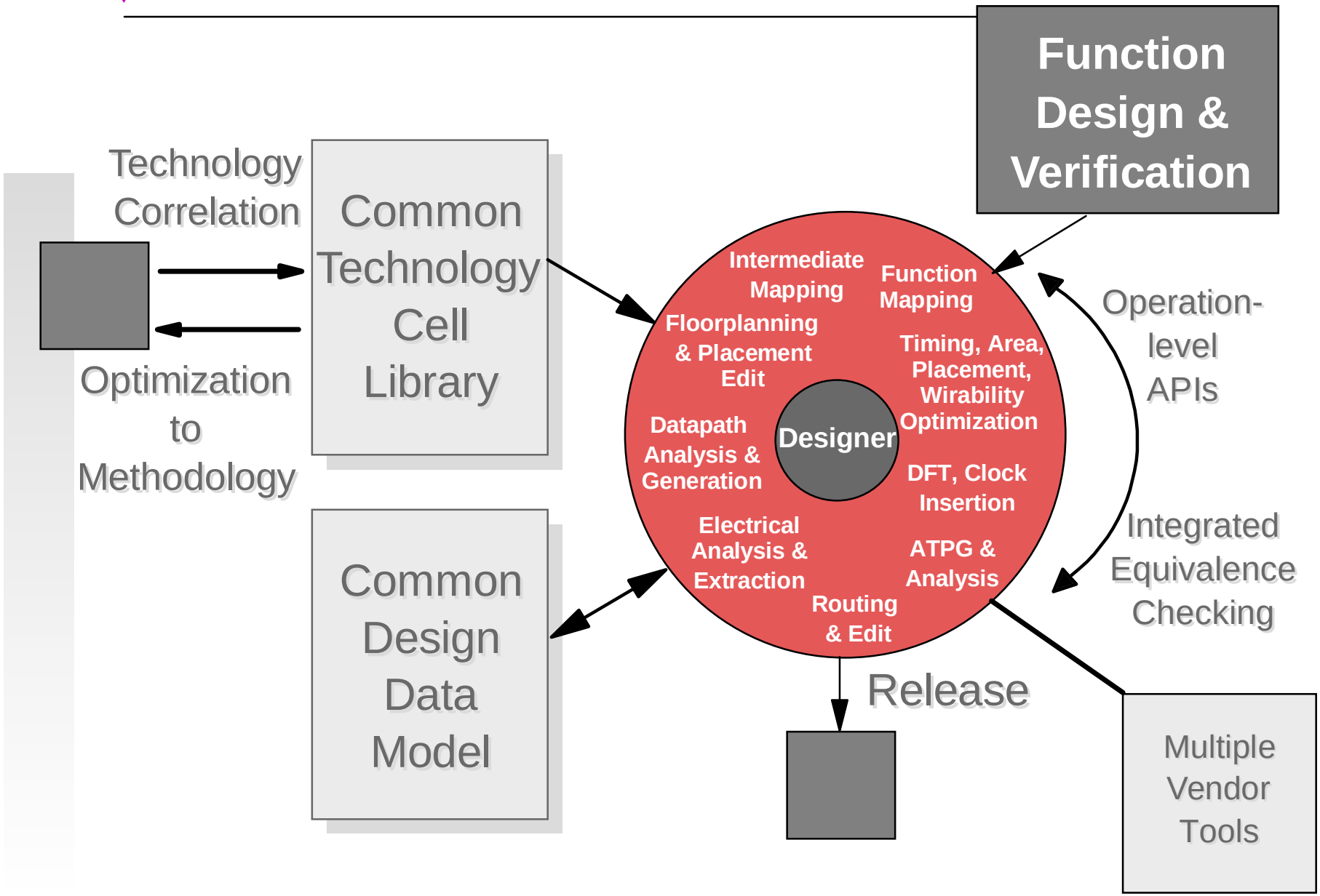
Post-handoff model



Pre-handoff model



Integrated Design Operations



Conclusions

- A major anticipated benefit of placement - based synthesis is TAT reduction
  - Reduction in schedule loops
- Methodology Integration
  - ASIC design methodology flow can exploit placement-based synthesis
  - Applicable in early synthesis and as a late timing closure method
  - Multi-vendor flows can be accommodated
- A complete integrated & interoperable flow is needed